19-5656; Rev 0; 12/10

# MAX9530 Evaluation Kit

Evaluates: MAX9530

## General Description

The MAX9530 evaluation kit (EV kit) provides a proven design to evaluate the MAX9530 quad NTSC/PAL decoder and quad audio codec. The EV kit also includes Windows XP®-, Windows Vista®-, and Windows® 7-compatible software that provides a graphical user interface (GUI) for exercising the features of the IC.

The EV kit comes with a MAX9530CXV+ installed.

## Features

- **Accepts Single-Ended or Differential Video**
- **Accepts Single-Ended or Differential Audio**
- **On-Board Frame Buffer Memory**
- **Digital Output Routing Through FPGA**
- **Digital Outputs Directly Drive FMC Connector**
- **Analog Audio Output Buffers**
- **Analog Video DAC**
- **Serial Digital Video Output Buffer at 270Mbps**
- **Windows XP-, Windows Vista-, and Windows 7-Compatible Software**
- **USB-PC Connection (Cable Included)**
- **Proven PCB Layout**
- **Fully Assembled and Tested**
- **Requires Single 5V Power Supply**

## Ordering Information

| PART | TYPE |
|---|---|
| MAX9530EVKIT+ | EV Kit |

*+Denotes lead(Pb)-free and RoHS compliant.*

## Component List

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| 5V_IN, PGND | 2 | Banana jacks |
| AIN1–AIN4, AOUT1, AOUT2 | 6 | Right-angle RCA jacks, white |
| AIN1N–AIN4N, AIN1P–AIN4P, GNDA, GNDV, VIN1N–VIN4N, VIN1P–VIN4P | 18 | 20G tinned copper bus wire into U-shape loops (0.25in off the PCB) |
| C1–C11, C212, C219, C220, C221, C223 | 0 | Not installed, ceramic capacitors (0603) |
| C12, C13 | 2 | 27pF ±5%, 50V C0G ceramic capacitors (0603) TDK C1608C0G1H270J |
| C14–C21, C66, C100–C104, C111, C121, C122 | 17 | 0.1µF ±10%, 25V X7R ceramic capacitors (0603) TDK C1608X7R1E104K |
| C22–C45, C47, C50, C73 | 27 | 0.1µF ±10%, 6.3V X5R ceramic capacitors (0201) TDK C0603X5R0J104K |
| C46, C49, C71 | 3 | 0.01µF ±10%, 6.3V X5R ceramic capacitors (0201) Murata GRM033R60J103K |
| C48, C51, C60, C61, C74, C108, C131, C141, C550, C551, C560, C561 | 12 | 1µF ±10%, 16V X7R ceramic capacitors (0603) TDK C1608X7R1C105K |
| C52–C59 | 8 | 0.47µF ±10%, 25V X7R ceramic capacitors (0603) Murata GRM188R71E474K |
| C62, C64, C65, C67, C69, C70, C72 | 7 | 2.2µF ±10%, 10V X7R ceramic capacitors (0603) Murata GRM188R71A225K |

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# MAX9530 Evaluation Kit

## Component List (continued)

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| C63, C68 | 2 | 470pF ±5%, 50V C0G ceramic capacitors (0603) TDK C1608C0G1H471J |
| C105 | 1 | 0.01µF ±10%, 16V X7R ceramic capacitor (0402) Murata GRM155R71C103K |
| C106, C107 | 2 | 22pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H220J |
| C109, C132, C142 | 3 | 10µF ±10%, 6.3V X7R ceramic capacitors (0805) Murata GRM21BR70J106K |
| C110 | 1 | 0.033µF ±10%, 25V X7R ceramic capacitor (0603) Murata GRM188R71E333K |
| C123, C124 | 2 | 10pF ±5%, 50V C0G ceramic capacitors (0603) Murata GRM1885C1H100J |
| C201, C202 | 2 | 10µF ±10%, 25V X5R ceramic capacitors (1206) Murata GRM31CR61E106K |
| C203 | 0 | Not installed, ceramic capacitor (1206) |
| C204, C205 | 2 | 330µF, 2.5V polymer capacitor (C case) SANYO 2R5TPE330MCC2 |
| C206 | 1 | 0.33µF ±10%, 10V X5R ceramic capacitor (0603) Murata GRM188R61A334K |
| C207, C208, C209, C213–C217 | 8 | 10µF ±20%, 6.3V X5R ceramic capacitors (0603) Murata GRM188R60J106M |
| C210, C218 | 2 | 1µF ±10%, 6.3V X5R ceramic capacitors (0603) Murata GRM188R60J105K |
| C211, C268 | 2 | 0.1µF ±10%, 25V X7R ceramic capacitors (0603) Murata GRM188R71E104K |
| C222, C267 | 2 | 1000pF ±10%, 50V X7R ceramic capacitors (0603) Murata GRM188R71H102K |
| C251–C266 | 16 | 0.047µF ±10%, 25V X7R ceramic capacitors (0603) TDK C1608X7R1E473K |
| C301–C304, C311–C314, C406, C407 | 10 | 0.1µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C104K |
| C401, C402 | 2 | 2.2µF ±10%, 6.3V X7R ceramic capacitors (0603) TDK C1608X5R0J225K |
| C403 | 1 | 0.01µF ±10%, 16V X7R ceramic capacitor (0603) Murata GRM188R71C103K |
| C404 | 1 | 4.7µF ±10%, 6.3V X5R ceramic capacitor (0603) TDK C1608X5R0J475K |
| C501–C526 | 26 | 1000pF ±10%, 25V X7R ceramic capacitors (0402) TDK C1005X7R1E102K |
| C531–C548 | 18 | 0.047µF ±10%, 16V X7R ceramic capacitors (0402) TDK C1005X7R1C473K |
| C600 | 1 | 10µF ±20%, 16V X5R ceramic capacitors (1206) Murata GRM31CR61C106M |
| C601–C608, C610 | 9 | 0.1µF ±10%, 16V X7R ceramic capacitors (0603) Murata GRM188R71C104K |
| D201 | 0 | Not installed, Schottky diode (SMA) |
| D202, D203 | 2 | Green LEDs (0603) |
| EXTCLK | 1 | 75Ω BNC PCB vertical mount |
| FB1, L101, L600 | 3 | Ferrite beads (0603) TDK MMZ1608R301A |
| H120, H123 | 0 | Not installed, 9-pin headers |
| H300 | 1 | 36-pin (2 x 18) header |

## Component List (continued)

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| H350 | 1 | FMC connector, low-density, 0.050in pitch socket array Samtec ASP-134603-01 |
| H501, H503 | 2 | 16-pin (2 x 8) headers |
| H502 | 1 | 26-pin (2 x 13) header |
| H600 | 1 | 2-pin header |
| JTAGU1, JTAGU120 | 0 | Not installed, 10-pin (2 x 5) headers |
| JTAGU500 | 1 | 6-pin header |
| JU1–JU24, JU26–JU30, JU201, JU203–JU209, JU350, JU500, JU501, JU502, JU506, JU507, JU550, JU551, JU560, JU561, JU601, JU602, JU603 | 50 | 2-pin headers |
| JU101–JU108 | 0 | Not installed, 2-pin headers—shorted with PCB trace |
| JU202, JU600 | 2 | 3-pin headers |
| JU25, JU31 | 2 | 5-pin headers |
| L200 | 1 | 1.4µH ±30%, 12A, 3.4M inductor Sumida CDEP105NP-1R4 |
| LED503, LED504 | 2 | Red LEDs (0805) |
| LEDPWR | 1 | Red LED (0805) |
| N201 | 1 | n-channel MOSFET (8 SO) Fairchild FDMS7692 |
| N202 | 1 | n-channel MOSFET (8 SO) Fairchild FDMS8660S |
| N203 | 0 | Not installed, dual MOSFET (8 SO) |
| NSOUT, SOUT | 2 | SMA connectors |
| PGOOD1, PGOOD2 | 0 | Not installed, multipurpose test points |
| Q100 | 1 | p-channel MOSFET (SOT223) Fairchild NDT456P |
| R1–R11 | 11 | 0Ω ±5% resistors (0603) |
| R12–R16, R18, R209–R212, R214–R220 | 0 | Not installed, resistors (0603) R209–R212 are shorted with PCB trace; all others are open |
| R17, R36–R51, R54, R55, R56, R60, R61, R62, R64–R67, R71 | 28 | 4.7kΩ ±5% resistors (0603) |
| R19 | 1 | 49.9kΩ ±1% resistor (0603) |
| R20–R35, R608–R613, R561 | 23 | 37.4Ω ±1% resistors (0603) |
| R52, R53, R57, R58, R59, R63, R213 | 7 | 10Ω ±5% resistors (0603) |
| R68, R72, R112, R500, R501, R502 | 6 | 10kΩ ±5% resistors (0603) |
| R69, R70 | 2 | 22Ω ±5% resistors (0402) |
| R100, R202, R203 | 3 | 1kΩ ±5% resistors (0603) |
| R101, R102 | 2 | 27Ω ±5% resistors (0603) |
| R103 | 1 | 1.5kΩ ±5% resistor (0603) |
| R104, R504 | 2 | 470Ω ±5% resistors (0603) |
| R111 | 1 | 2.2kΩ ±5% resistor (0603) |
| R201 | 1 | 0.002Ω ±1% resistor (2010) Vishay WSL20102L000FEA |
| R204–R207, R600, R601 | 6 | 100kΩ ±5% resistors (0603) |
| R208 | 1 | 200kΩ ±1% resistor (0603) |
| R401, R402 | 2 | 75Ω ±1% resistors (0603) |
| R403, R404 | 2 | 110Ω ±1% resistors (0603) |
| R405, R406 | 2 | 232Ω ±1% resistors (0603) |
| R503 | 1 | 680Ω ±5% resistor (0603) |
| R505, R506, R507 | 3 | 4.7kΩ ±5% resistors (0603) |
| R562 | 1 | 75kΩ ±1% resistor (0603) |
| R602 | 1 | 150Ω ±5% resistor (0603) |
| R603, R605, RTCK, RTDI, RTDO, RTMS | 6 | 100Ω ±5% resistors (0603) |
| R604 | 1 | 4.02kΩ ±1% resistor (0603) |
| R606, R607, R615, R616, R617 | 5 | 75Ω ±5% resistors (0603) |
| RLEDPWR | 1 | 330Ω ±5% resistor (0603) |

# MAX9530 Evaluation Kit

## Component List (continued)

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| RN1–RN6 | 6 | 22Ω ±2% x 8 independent resistors array (0402 x 8 convex) Panasonic EXB-2HV220JV |
| SW_RESET | 1 | Momentary NO switch |
| TP3–TP8 | 6 | White multipurpose test points |
| TP00, TP100, TP101, TP108, TP132, TP142 | 0 | Not installed, multipurpose test points |
| TP201, TP202 | 2 | Red multipurpose test points |
| TP403, TP404, TP405 | 0 | Not installed, multipurpose test points |
| U/BLUE, V/RED, Y/GREEN | 3 | Right-angle RCA jacks |
| U1 | 1 | Video and audio encoder (CSBGA 196) Maxim MAX9530CXV+ |
| U2 | 1 | Dual op amp, 5V single-supply unity-gain-stable (8 SOT23) Maxim LMX358AKA+ (Top Mark: AAIR) |
| U100 | 1 | UART-to-USB converter (32 TQFP) |
| U110 | 1 | 93C46 type 3-wire EEPROM 16-bit architecture (8 SO) |
| U120 | 1 | Low-power microcontroller (68 QFN-EP) Maxim MAXQ2000-RAX+ |
| U130 | 1 | 2.5V regulator (5 SC70) Maxim MAX8511EXK25+T (Top Mark: ADV) |
| U140 | 1 | 3.3V regulator (5 SC70) Maxim MAX8511EXK33+T (Top Mark: AEI) |

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| U200 | 1 | Maxim complete power solution for DDR, DDR2, and DDR3 memory (24 TQFN) Maxim MAX17000ETG+ |
| U250 | 1 | 360MHz DDR2 memory, 4M x 16 x 4 (84 FBGA) Micron MT47H16M16BG-37E:B |
| U300, U310 | 2 | Low-voltage TTL buffers (48 TSSOP) |
| U400 | 1 | SMPTE 259M 270MHz cable driver National Semi CLC006 |
| U500 | 1 | FPGA, Spartan-3AN, 200k, nonvolatile configuration (256 FBGA) Xilinx XC3S200AN-5FTG256C |
| U500TCK, U500TDI, U500TDO, U500TMS | 4 | White multipurpose test points |
| U550, U560 | 2 | 3.3V, 1000mA LDO regulators (16 TSSOP-EP) Maxim MAX8869EUE33+ |
| U600 | 1 | Digital PAL/NTSC video encoder (44 MQFP) Analog Devices ADV7171KSZ |
| U610 | 1 | Triple standard-definition video filter amplifier (8 µMAX®) Maxim MAX9584AUA+ |
| USB1 | 1 | USB type-B right-angle female receptacle |
| VIN1–VIN4 | 4 | Right-angle RCA jacks, yellow |

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## Component List (continued)

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| Y1 | 1 | 27MHz crystal, fundamental mode Hong Kong X'tals SSM27000N1HK188F0-0 |
| Y100 | 1 | 6MHz crystal (HCM49) Hong Kong X'tals SSL60000N1HK188F0-0 |
| Y120 | 1 | 16MHz crystal (HCM49) Hong Kong X'tals SSM16000N1HK188F0-0 |

| DESIGNATION | QTY | DESCRIPTION |
|---|---|---|
| — | 1 | USB high-speed A-to-B cables, 6ft |
| — | 0 | Not included: FMC cable Samtec ASP-134603-01 |
| — | 40 | Shunts |
| — | 1 | PCB: MAX9530 EVALUATION KIT+ |

## Component Suppliers

| SUPPLIER | PHONE | WEBSITE |
|---|---|---|
| Fairchild Semiconductor | 888-522-5372 | www.fairchildsemi.com |
| Hong Kong X'tals Ltd. | 852-35112388 | www.hongkongcrystal.com |
| Murata Electronics North America, Inc. | 770-436-1300 | www.murata-northamerica.com |
| Samtec, Inc. | 800-726-8329 | www.samtec.com |
| SANYO Electric Co., Ltd. | 619-661-6835 | www.sanyo.com |
| Sumida Corp. | 847-545-6700 | www.sumida.com |
| TDK Corp. | 847-803-6100 | www.component.tdk.com |
| Vishay | 402-563-6866 | www.vishay.com |

***Note:*** *Indicate that you are using the MAX9530 when contacting these component suppliers.*

## MAX9530 EV Kit Files

| FILE | DESCRIPTION |
|---|---|
| INSTALL.EXE | Installs the EV kit files on your computer |
| MAX9530.EXE | Application program |
| FTD2XX.INF | USB device driver file |
| CDM20600.EXE | Installs the USB device driver |
| UNINSTALL.EXE | Uninstalls the EV kit software |
| USB_Driver_Help_200.PDF | USB driver installation help file |

# MAX9530 Evaluation Kit

## Quick Start

### Required Equipment

- MAX9530 EV kit (USB cable included)
- Windows XP, Windows Vista, or Windows 7 PC with a spare USB port
- User-supplied 5V DC at 1000mA power supply
- User-supplied standard-definition video display

**Note:** In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

### Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation:

1) Visit www.maxim-ic.com/evkitsoftware to download the latest version of the EV kit software, 9530Rxx.ZIP. Save the EV kit software to a temporary folder and uncompress the ZIP file.
2) Install the EV kit software and USB driver on your computer by running the INSTALL.EXE program inside the temporary folder. The program files are copied to your PC and icons are created in the Windows **Start | Programs** menu. During software installation, some versions of Windows may show a warning message indicating that this software is from an unknown publisher. This is not an error condition and it is safe to proceed with installation. Administrator privileges are required to install the USB device driver on Windows.
3) Verify that all jumpers are in their default positions, as shown in Tables 1–5.
4) Connect the 5V DC power supply to the 5V_IN and PGND banana jacks.
5) Connect the video display to the Y/GREEN RCA jack.
6) Connect the USB cable from the PC to the EV kit board. A Windows message appears when connecting the EV kit board to the PC for the first time. Each version of Windows has a slightly different message. If you see a Windows message stating **ready to use**, then proceed to the next step; otherwise, open the USB_Driver_Help_200.PDF document in the Windows **Start | Programs** menu to verify that the USB driver was installed successfully.
7) Start the EV kit software by opening its icon in the **Start | Programs** menu. The EV kit software main window appears, as shown in Figure 1. Wait as the software is **searching for hardware** and then for the software to load two default configuration files before proceeding.
8) *Color Bar Test:* On the **Video Decoder 1** tab sheet, scroll down to register **0x2B Test Pattern** and set **CBAR** to **10: 75% Color Bars**. Press the **Write** button. The video display shows 75% color bars.
9) *Quad Splitscreen Test (NTSC):* Configure a unique video signal for each of the four video inputs.
10) Select **File | Load Configuration File...** inside the **config_files** folder, and load file **max9530_scale-360-525_ovl.MAX9530**. The video display shows video signal 1 scaled to fit into the upper quadrant of the screen, and the rest of the video display is blank.
11) On the **FPGA** tab sheet, inside the **0x01 3xDAC (ADI) input selection** group box, check **four channel overlay** and remove the checks from **channel 4** through **channel 1**. The video display is reconfigured to show a split screen with four images from each of the four video decoders.
12) On the **Video Router** tab sheet, scroll to register **0x60 FIFO Source** and change the order from Vin4 – Vin3 – Vin2 – Vin1 and press the **Write** button. The new order is reflected in the video display. The channel selected by CH1R appears in the upper-left quadrant of the video display.

## Detailed Description of Software

The **Read All** button reads all the MAX9530 device registers. **Reset to Default Values** restores recommended factory settings, and **Write All** writes all device registers with the values shown in the GUI.

The **Status** tab sheet (Figure 1) provides direct access to all the registers of the device. Each register has its own **Read** and **Write** buttons. The small circle next to the **Read** button turns yellow to indicate an attempt to read or write, red to indicate a failed read or write, and green to indicate a successful read or write operation. The other tab sheets work similarly. The **Registers** tab sheet has all the IC's segment 0 registers, while the **Status**, **Video Decoder_**, **Video Router**, and **Audio** tab sheets each contain a subset of the device registers.

The **FPGA** tab sheet (Figure 3) controls the functions of the FPGA (U500). Register **0x01 3xDAC (ADI) input selection** selects which digital video data is sent to the U600 video DAC. Register **0x02 D1 Serial Digital Output** controls which digital video data is sent to connectors SOUT and NSOUT. The FPGA outputs a color bar test pattern if no channel is selected or if multiple bits are set. Register **0x03 Control Register** enables the serial video output buffer (SOUT/NSOUT driven by U400), selects the output format, and header H300 outputs. The optional I²S audio generator is enabled by the **I2S Audio Playback [SDIN, BCLKP, WCLKP]** field.

The **ITU Demultiplexer** tab sheet contains the U600 registers. If using a composite video monitor attached to Y/GREEN, scroll to **0x03 ADV7171 Mode Register 3** to set the **DAC Output** to **1: DAC.A=Grn/Luma/Y**, **DAC.D=Composite**, and then press the **Write** button.

### *Advanced User Interface*

There are two methods for communicating with the IC. The first is through the windows shown in Figures 1, 2, and 3, and the second is through the **Advanced User Interface** window shown in Figure 4. The **Advanced User Interface** window becomes available by selecting the **Options | Interface (Advanced User)** menu item and allows execution of serial commands manually.

The **Advanced User Interface** window can also be used as a debug tool because it is capable of manually reading and writing to every register of the IC.

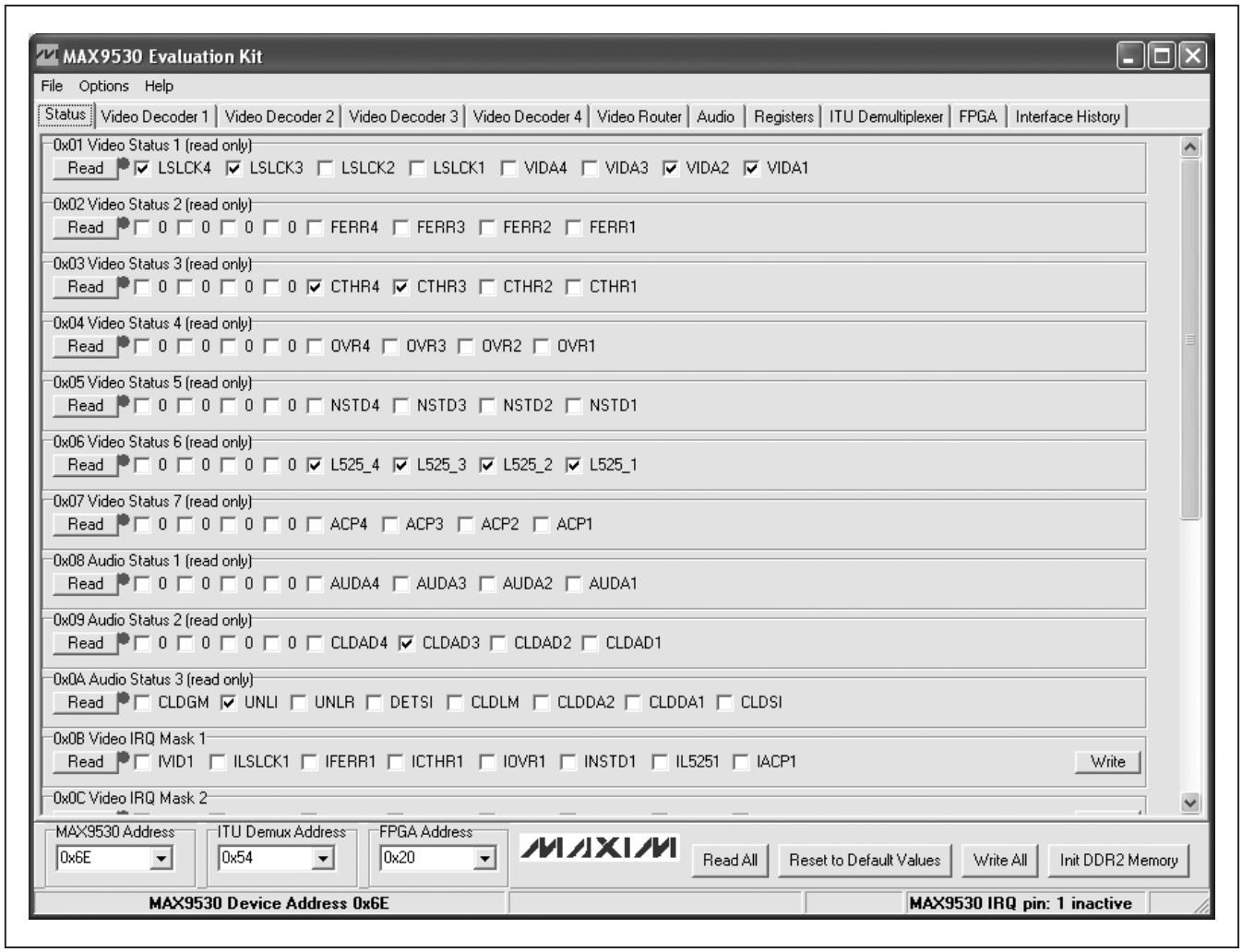


*Figure 1. MAX9530 EV Kit Software Main Window (Status Tab)*

# MAX9530 Evaluation Kit

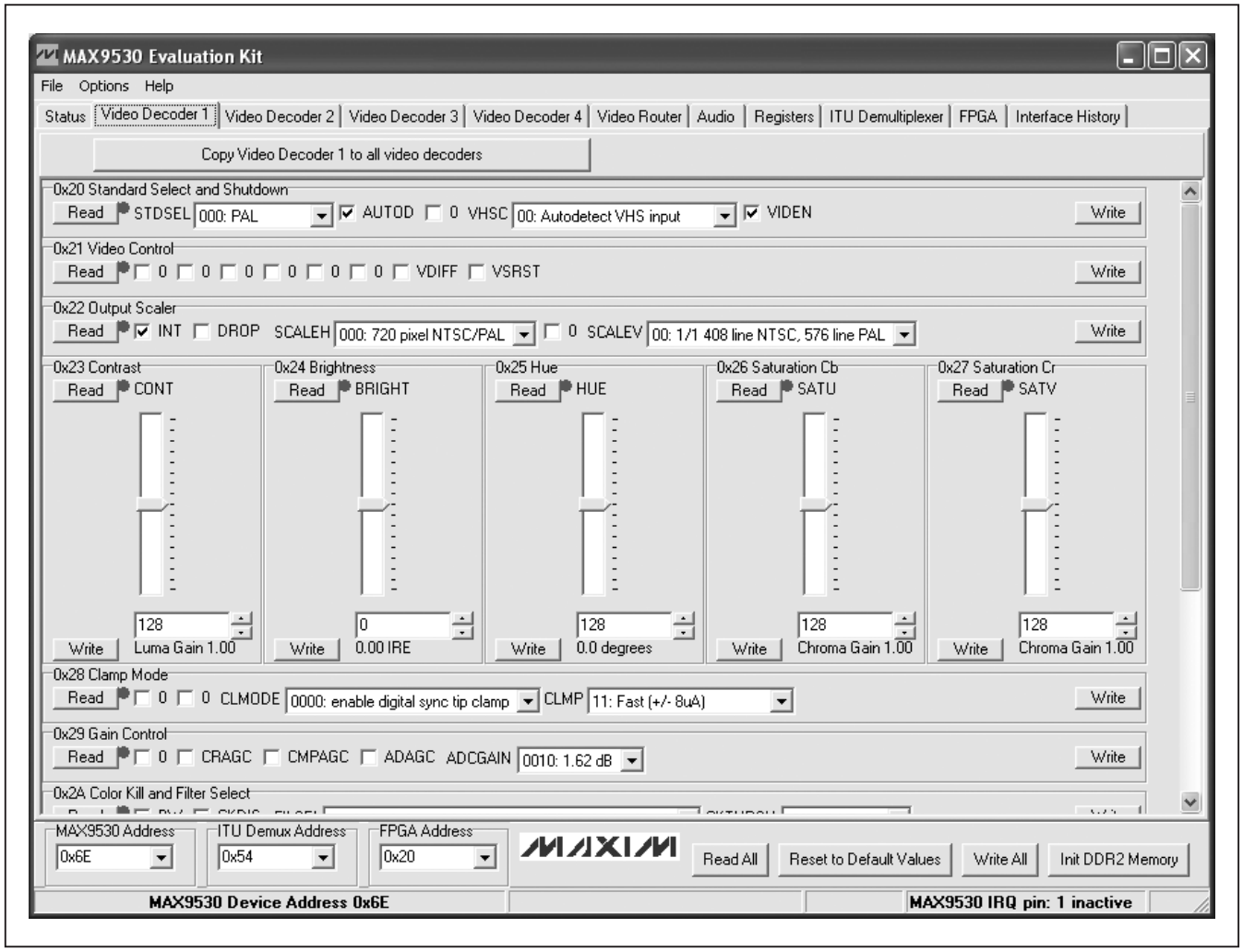


*Figure 2. MAX9530 EV Kit Software Main Window (Video Decoder 1 Tab)*

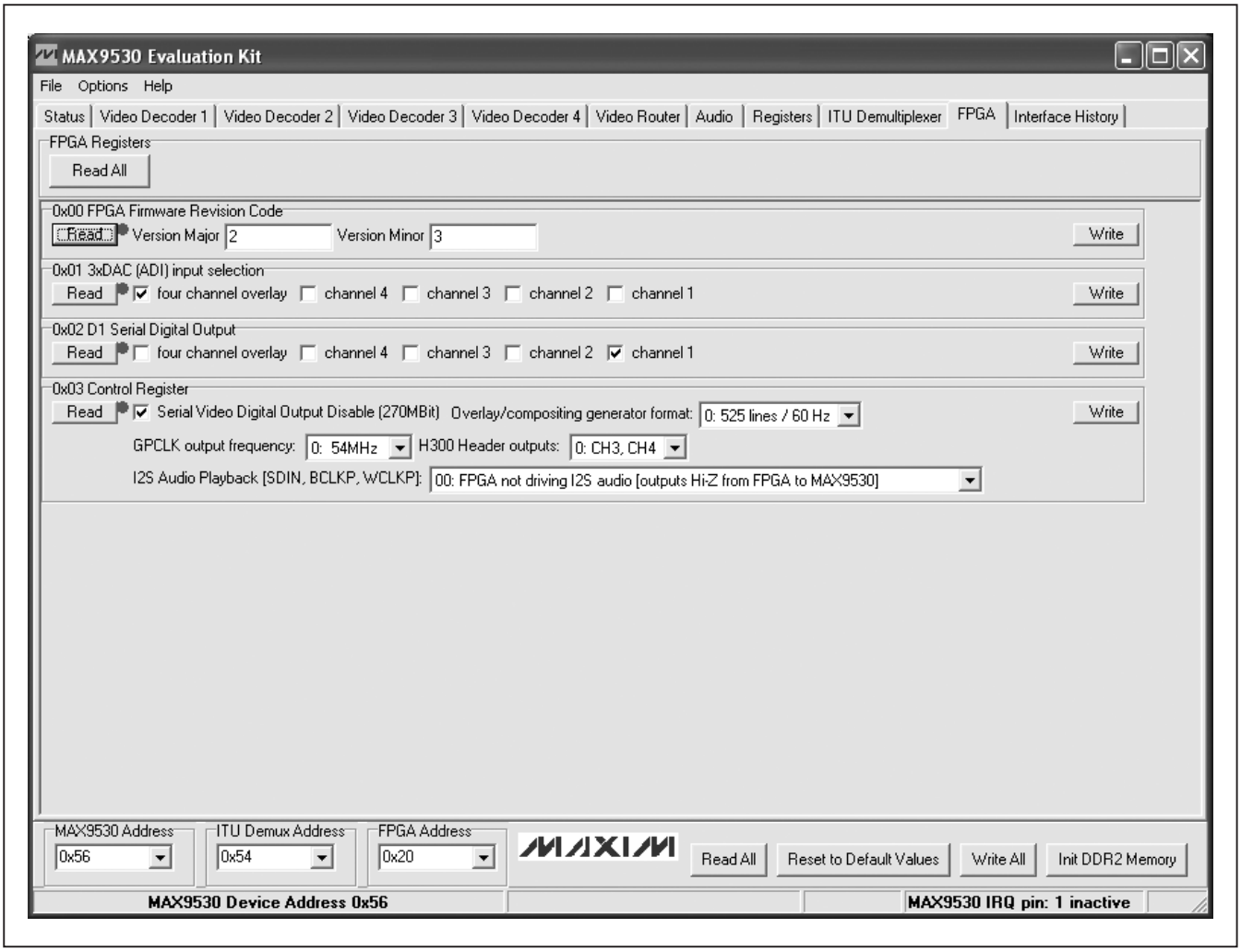


*Figure 3. MAX9530 EV Kit Software Main Window (FPGA Tab)*

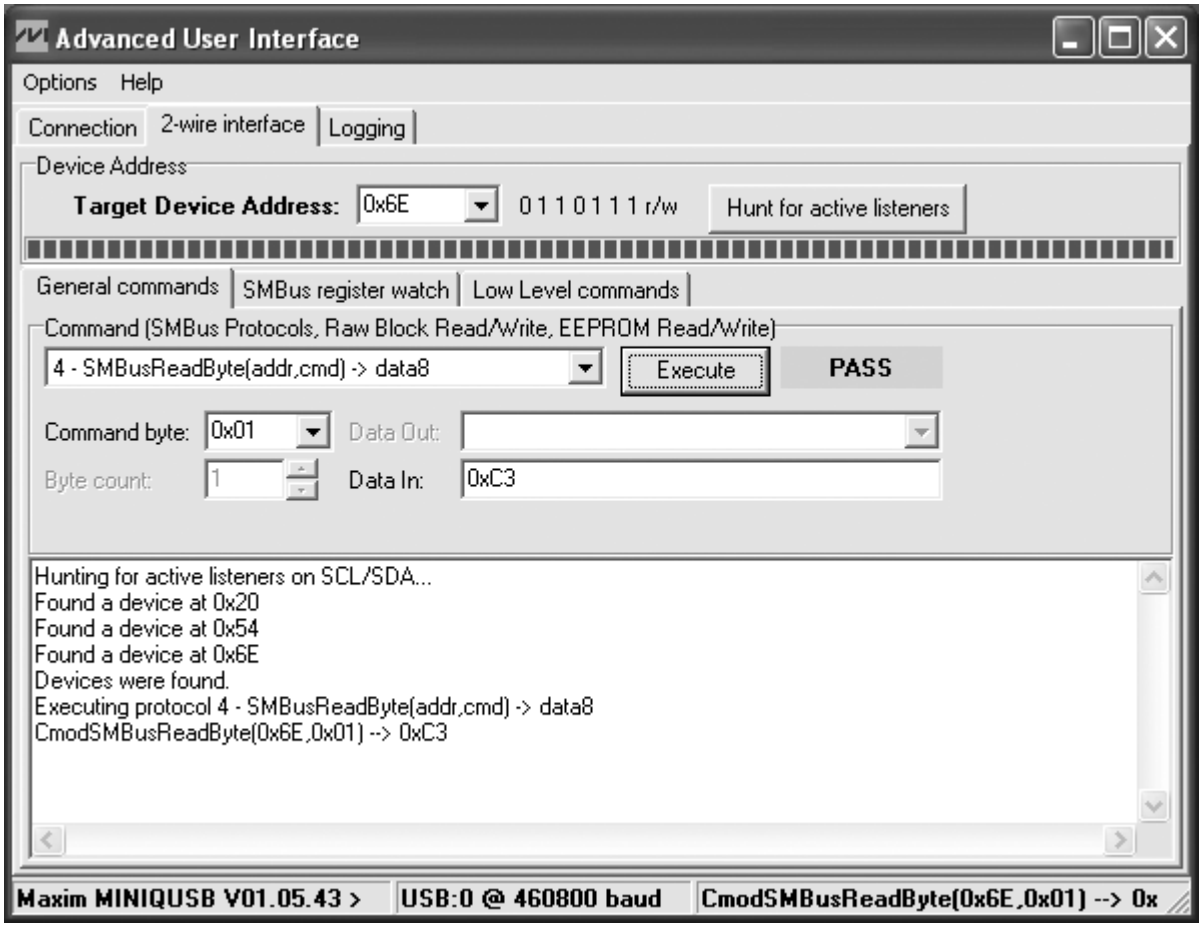


*Figure 4. Advanced User Interface Window (2-Wire Interface Tab)*

## _Detailed Description of Hardware

The MAX9530 EV kit provides a proven layout for the MAX9530. Frame buffer memory, multifunction FPGA, analog audio and video output buffers, and easy-to-use USB-PC connection are included on the EV kit.

Standard MINIQUSB-equivalent microcontroller circuits (U100, U110, U120, U130, and U140) connect from the USB to the I²C interface (H123). The MINIQUSB circuit powers its +2.5V and +3.3V supplies from the +5V USB.

External user-supplied +5V DC power connects to the board through banana jacks 5V_IN and PGND. The MAX17000 switching power supply (U200) supplies +1.8V and +0.9V to power the DDR2 memory (U250).

The FPGA (U500) routes the digital video and audio outputs to headers H501, H502, and H503. Additionally, digital video can be routed through serial video buffer U400 to SOUT/NSOUT. The FPGA can supply a digital audio test signal. Any channel (1–4) can be routed to the digital output headers or the analog video DAC (U600). Additionally, channels 1–4 can be composed into a quad split-screen display. For proper operation, the FPGA requires the 27MHz global clock output from U1 to be enabled.

## Table 1. Jumper Descriptions (JU1–JU31)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU1 | MCLKR | Open* | Optional connection point for driving or monitoring digital audio. |
| JU2 | SDOUT | Open* | Optional connection point for driving or monitoring digital audio. |
| JU3 | LRCLKR | Open* | Optional connection point for driving or monitoring digital audio. |
| JU4 | BCLKR | Open* | Optional connection point for driving or monitoring digital audio. |
| JU5 | SDOUTM | Open* | Optional connection point for driving or monitoring digital audio. |
| JU6 | SDIN | Open* | Optional connection point for driving or monitoring digital audio. |
| JU7 | LRCLKP | Open* | Optional connection point for driving or monitoring digital audio. |
| JU8 | BCLKP | Open* | Optional connection point for driving or monitoring digital audio. |
| JU9 | LRCLKAL | Open* | Optional connection point for driving or monitoring digital audio. |
| JU10 | BCLKAL | Open* | Optional connection point for driving or monitoring digital audio. |
| JU11 | SDIOAL | Open* | Optional connection point for driving or monitoring digital audio. |
| JU12 | REF27O | 1-2* | REF27O output drives the REF27I input. |
| | | Open | REF27I must be driven by an external user-supplied 27MHz. |
| JU13 | VIN1N | 1-2* | VIN1N = GND. Apply a single-ended signal to the VIN1 phono plug. |
| | | Open | Apply a differential signal between VIN1P and VIN1N. |
| JU14 | VIN2N | 1-2* | VIN2N = GND. Apply a single-ended signal to the VIN2 phono plug. |
| | | Open | Apply a differential signal between VIN2P and VIN2N. |
| JU15 | VIN3N | 1-2* | VIN3N = GND. Apply a single-ended signal to the VIN3 phono plug. |
| | | Open | Apply a differential signal between VIN3P and VIN3N. |
| JU16 | VIN4N | 1-2* | VIN4N = GND. Apply a single-ended signal to the VIN4 phono plug. |
| | | Open | Apply a differential signal between VIN4P and VIN4N. |
| JU17 | VDDIO | 1-2* | VDDIO = +3.3V. |
| | | Open | VDDIO must be driven by an external user-supplied power supply. |
| JU18 | VDDD | 1-2* | VDDD = +1.8V from the MAX17000 (U200). |
| | | Open | VDDD must be driven by an external user-supplied power supply. |
| JU19 | VDDA | 1-2* | VDDA = VDDD filtered by ferrite bead FB1. |
| | | Open | VDDA must be driven by an external user-supplied power supply. |
| JU20 | AIN1N | 1-2* | AIN1N = GND. Apply a single-ended signal to the AIN1 phono plug. |
| | | Open | Apply a differential signal between AIN1P and AIN1N. |
| JU21 | AIN2N | 1-2* | AIN2N = GND. Apply a single-ended signal to the AIN2 phono plug. |
| | | Open | Apply a differential signal between AIN2P and AIN2N. |
| JU22 | AIN3N | 1-2* | AIN3N = GND. Apply a single-ended signal to the AIN3 phono plug. |
| | | Open | Apply a differential signal between AIN3P and AIN3N. |
| JU23 | AIN4N | 1-2* | AIN4N = GND. Apply a single-ended signal to the AIN4 phono plug. |
| | | Open | Apply a differential signal between AIN4P and AIN4N. |
| JU24 | SCL | 1-2* | IC (U1) SCL is driven by the MAXQ2000 (U120). |
| | | Open | IC must be driven by an external user-supplied $I^2C$ master. |
| JU25 | DEVADDR1 | 1-2 | DEVADDR1 = VDDIO. |
| | | 1-3* | DEVADDR1 = SCL. |
| | | 1-4 | DEVADDR1 = GND. |
| | | 1-5 | DEVADDR1 = SDA. |

## Table 1. Jumper Descriptions (JU1–JU31) (continued)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU26 | SDA | 1-2* | IC (U1) SDA is driven by the MAXQ2000 (U120). |
| | | Open | IC must be driven by an external user-supplied I²C master. |
| JU27 | SCL pullup | 1-2* | R66 pulls up idle SCL to VDDIO. |
| | | Open | SCL requires an external user-supplied resistive pullup. |
| JU28 | SDA pullup | 1-2* | R67 pulls up idle SDA to VDDIO. |
| | | Open | SDA requires an external user-supplied resistive pullup. |
| JU29 | IRQB | 1-2* | IC (U1) IRQB drives the MAXQ2000 (U120) on the MINIQUSB GPIO pin K1. |
| | | Open | Connect IC (U1) IRQB to user-supplied controller. |
| JU30 | RSTB | 1-2* | IC (U1) RSTB is driven by the MAXQ2000 (U120) from the MINIQUSB GPIO pin K2. |
| | | Open | Drive IC (U1) RSTB from a user-supplied controller. |
| JU31 | DEVADDR0 | 1-2 | DEVADDR0 = VDDIO. |
| | | 1-3* | DEVADDR0 = SCL. |
| | | 1-4 | DEVADDR0 = GND. |
| | | 1-5 | DEVADDR0 = SDA. |

**Default position.*

## Table 2. Jumper Descriptions (JU201–JU209)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU201 | U200 OVP | 1-2 | MAX17000 (U200) OVP = AGND. Overvoltage protection is disabled. |
| | | Open* | MAX17000 (U200) OVP = VDD. Overvoltage protection is enabled. |
| JU202 | U200 FB | 1-2* | MAX17000 (U200) FB connects to VDD. VOUT = +1.8V. |
| | | 2-3 | MAX17000 (U200) FB connects to GND. VOUT = +1.5V. |
| | | Open | MAX17000 (U200) FB connects to resistive-dividers R214/R215. Refer to the MAX17000 IC data sheet. |
| JU203 | U200 $\overline{\text{STDBY}}$ | 1-2 | MAX17000 (U200) $\overline{\text{STDBY}}$ = GND. VTT is disabled (U250 DDR2 memory not powered). |
| | | Open* | MAX17000 (U200) $\overline{\text{STDBY}}$ = VDD. VTT = +0.9V. Normal operation of DDR2 memory. |
| JU204 | U200 $\overline{\text{SKIP}}$ | 1-2 | MAX17000 (U200) $\overline{\text{SKIP}}$ = GND. Pulse-skipping mode is enabled. |
| | | Open* | MAX17000 (U200) $\overline{\text{SKIP}}$ = VDD. Forced-PWM operation mode, no pulse-skipping. |
| JU205 | U200 $\overline{\text{SHDN}}$ | 1-2 | MAX17000 (U200) $\overline{\text{SHDN}}$ = GND. VOUT is disabled (U250 DDR2 memory is not powered). |
| | | Open* | MAX17000 (U200) $\overline{\text{SHDN}}$ = VDD. VOUT = +1.8V. Normal operation of DDR2 memory. |
| JU206 | U200 REFIN | 1-2* | MAX17000 (U200) REFIN = VDD. VTT = VCSL/2. |
| | | Open | Refer to the MAX17000 IC data sheet. |

## Table 2. Jumper Descriptions (JU201–JU209) (continued)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU207 | U200_VDD | 1-2* | MAX17000 (U200) VDD is supplied by +5V. |
| | | Open | Current meter connection. |
| JU208 | +5V | 1-2* | +5V is supplied from an external user-supplied power at the 5V_IN banana jack. |
| | | Open | Current meter connection. |
| JU209 | U200 IN | 1-2* | MAX17000 (U200) IN is supplied by +5V. |
| | | Open | Current meter connection. |

**Default position.*

## Table 3. Jumper Description (JU350)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU350 | H350 3.3V | 1-2* | H350 3P3V and 3P3VAUX are driven with +3.3V supplied by U550 through JU551. |
| | | Open | H350 3P3V and 3P3VAUX are unconnected. |

## Table 4. Jumper Descriptions (JU500, JU501, JU502, JU506, JU507, JU550, JU551, JU560, JU561)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU500 | U500 M0 | 1-2 | FPGA (U500) mode select M0 = 0. |
| | | Open* | FPGA (U500) mode select M0 = 1. |
| JU501 | U500 M1 | 1-2 | FPGA (U500) mode select M1 = 0. |
| | | Open* | FPGA (U500) mode select M1 = 1. |
| JU502 | U500 M2 | 1-2* | FPGA (U500) mode select M2 = 0. |
| | | Open | FPGA (U500) mode select M2 = 1. |
| JU506 | U500 PROG_B | 1-2 | FPGA (U500) PROG_B = 0. |
| | | Open* | FPGA (U500) PROG_B = 1. |
| JU507 | U500 SUSPEND | 1-2 | FPGA (U500) SUSPEND = 0. |
| | | Open* | FPGA (U500) SUSPEND = 1. |
| JU550 | U550 IN | 1-2* | MAX8869 regulator (U550) is powered by +5V. |
| | | Open | Current meter connection. |
| JU551 | U550 OUT | 1-2* | MAX8869 regulator (U550) regulator drives +3.3V. |
| | | Open | Current meter connection. |
| JU560 | U560 IN | 1-2* | MAX8869 regulator (U560) regulator is powered by +3.3V. |
| | | Open | Current meter connection. |
| JU561 | U560 OUT | 1-2* | MAX8869 regulator (U560) regulator drives +1.2V. |
| | | Open | Current meter connection. |

**Default position.*

## Table 5. Jumper Descriptions (JU600–JU603)

| JUMPER | SIGNAL | SHUNT POSITION | DESCRIPTION |
|---|---|---|---|
| JU600 | U600 ALSB | 1-2 | ADV7171A (U600) ALSB = 1. Device address = 0x56.<br>(Be sure to set JU25 and JU31 to avoid address conflict with the IC.) |
| | | 2-3* | ADV7171A (U600) ALSB = 0. Device address = 0x54.<br>(Be sure to set JU25 and JU31 to avoid address conflict with the IC.) |
| JU601 | U600 $\overline{\text{HSYNC}}$ | 1-2 | ADV7171A (U600) $\overline{\text{HSYNC}}$ = GND. |
| | | Open* | ADV7171A (U600) $\overline{\text{HSYNC}}$ = Open. |
| JU602 | U600 FIELD $\overline{\text{SYNC}}$ | 1-2 | ADV7171A (U600) FIELD$\overline{\text{SYNC}}$ = GND. |
| | | Open* | ADV7171A (U600) FIELD$\overline{\text{SYNC}}$ = Open. |
| JU603 | U600 $\overline{\text{BLANK}}$ | 1-2 | ADV7171A (U600) $\overline{\text{BLANK}}$ = GND. |
| | | Open* | ADV7171A (U600) $\overline{\text{BLANK}}$ = Open. |

**Default position.*

## Table 6. U1 Device Address Select Jumper Descriptions (JU25, JU31)

| JU25 | | JU31 | | I²C DEVICE ADDRESS |
|---|---|---|---|---|
| SHUNT POSITION | DEVADDR1 | SHUNT POSITION | DEVADDR0 | |
| 1-2 | VDDIO | 1-2 | VDDIO | 0x56 |
| 1-2 | VDDIO | 1-3 | SCL | 0x5E |
| 1-2 | VDDIO | 1-4 | GND | 0x54 |
| 1-2 | VDDIO | 1-5 | SDA | 0x5C |
| 1-3 | SCL | 1-2 | VDDIO | 0x6A |
| 1-3* | SCL | 1-3* | SCL | 0x6E |
| 1-3 | SCL | 1-4 | GND | 0x68 |
| 1-3 | SCL | 1-5 | SDA | 0x6C |
| 1-4 | GND | 1-2 | VDDIO | 0x52 |
| 1-4 | GND | 1-3 | SCL | 0x5A |
| 1-4 | GND | 1-4 | GND | 0x50 |
| 1-4 | GND | 1-5 | SDA | 0x58 |
| 1-5 | SDA | 1-2 | VDDIO | 0x62 |
| 1-5 | SDA | 1-3 | SCL | 0x66 |
| 1-5 | SDA | 1-4 | GND | 0x60 |
| 1-5 | SDA | 1-5 | SDA | 0x64 |

**Default position.*

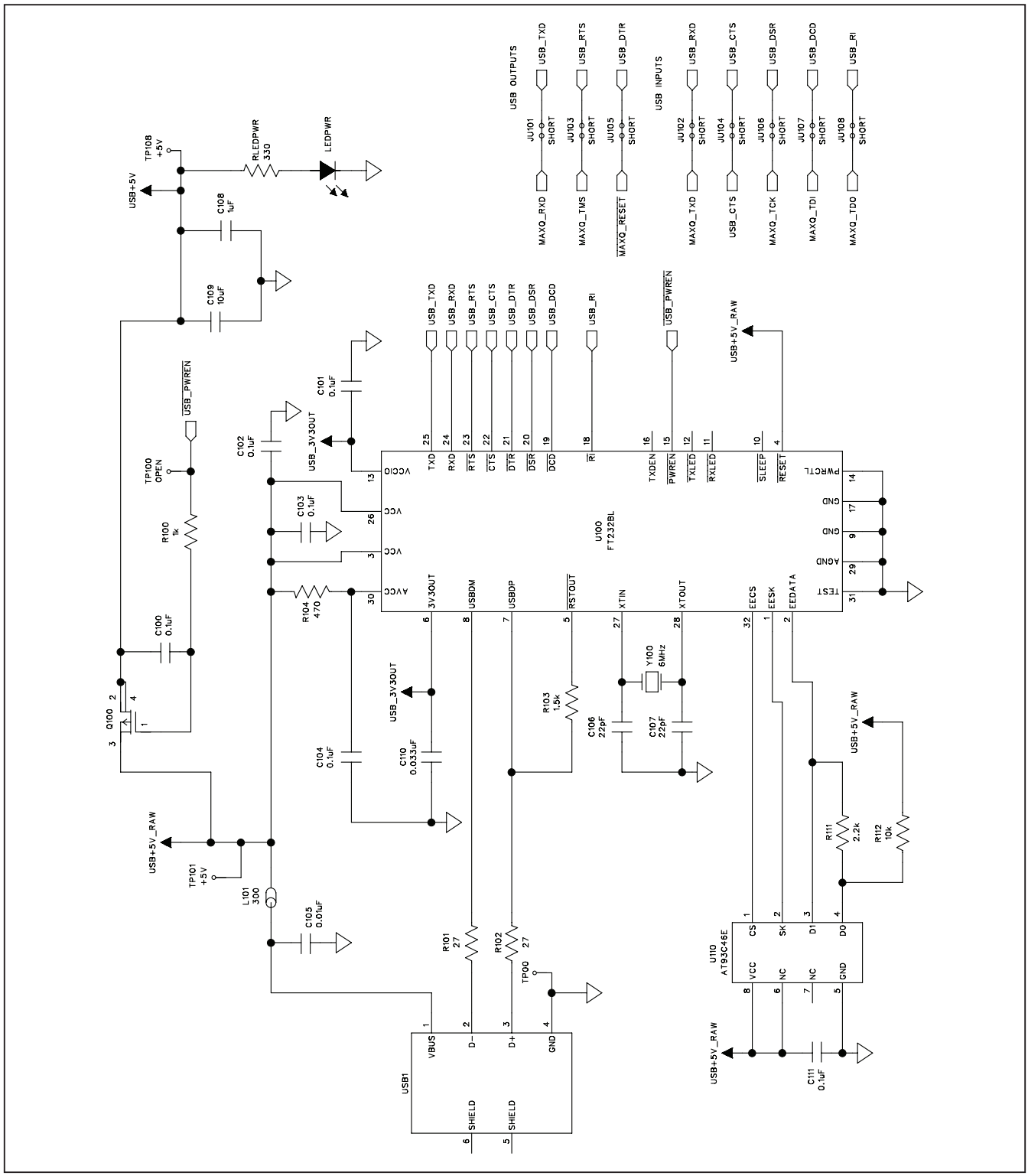


*Figure 5a. MAX9530 EV Kit Schematic (Sheet 1 of 13)*

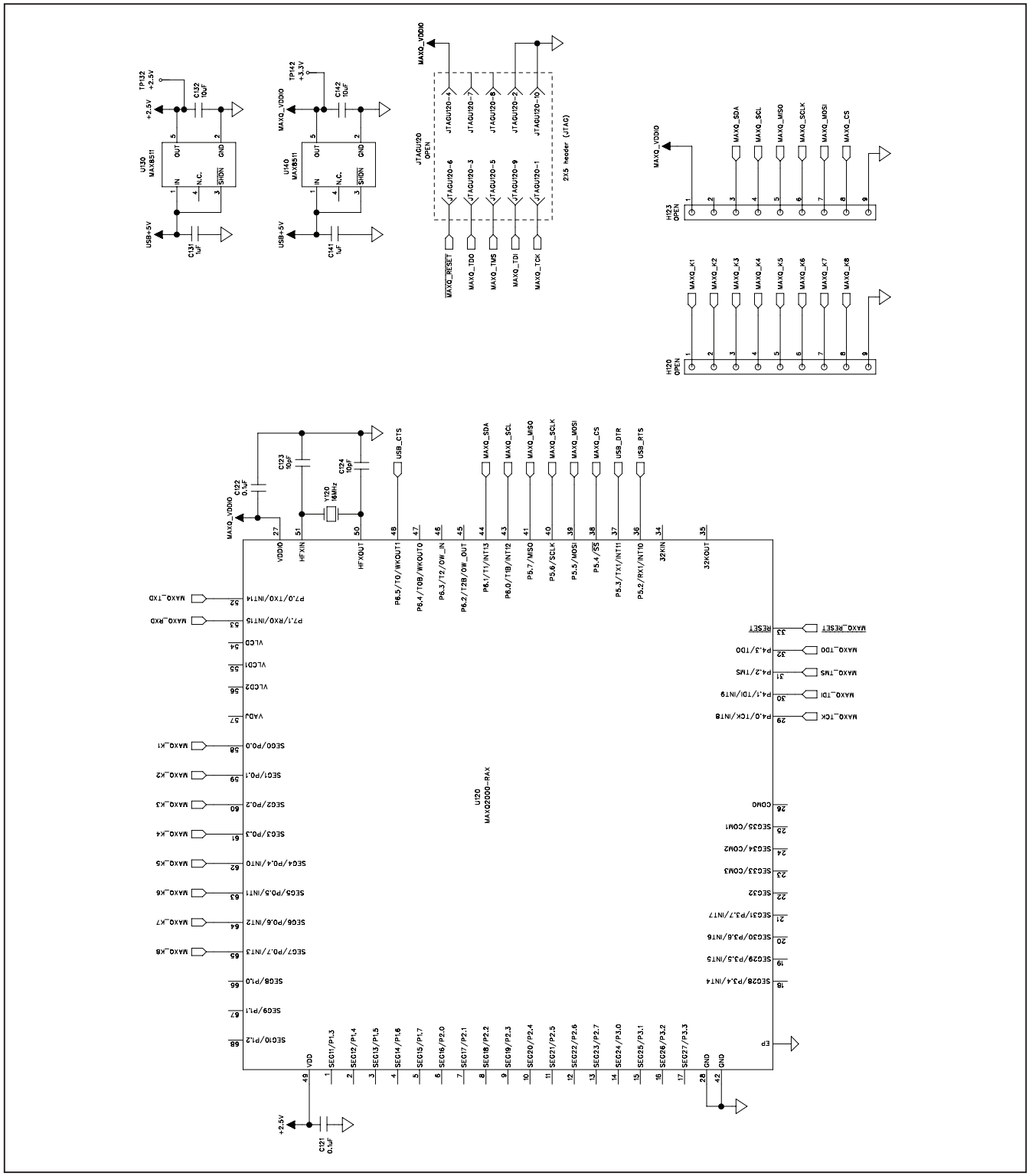

Figure 5b. MAX9530 EV Kit Schematic (Sheet 2 of 13)

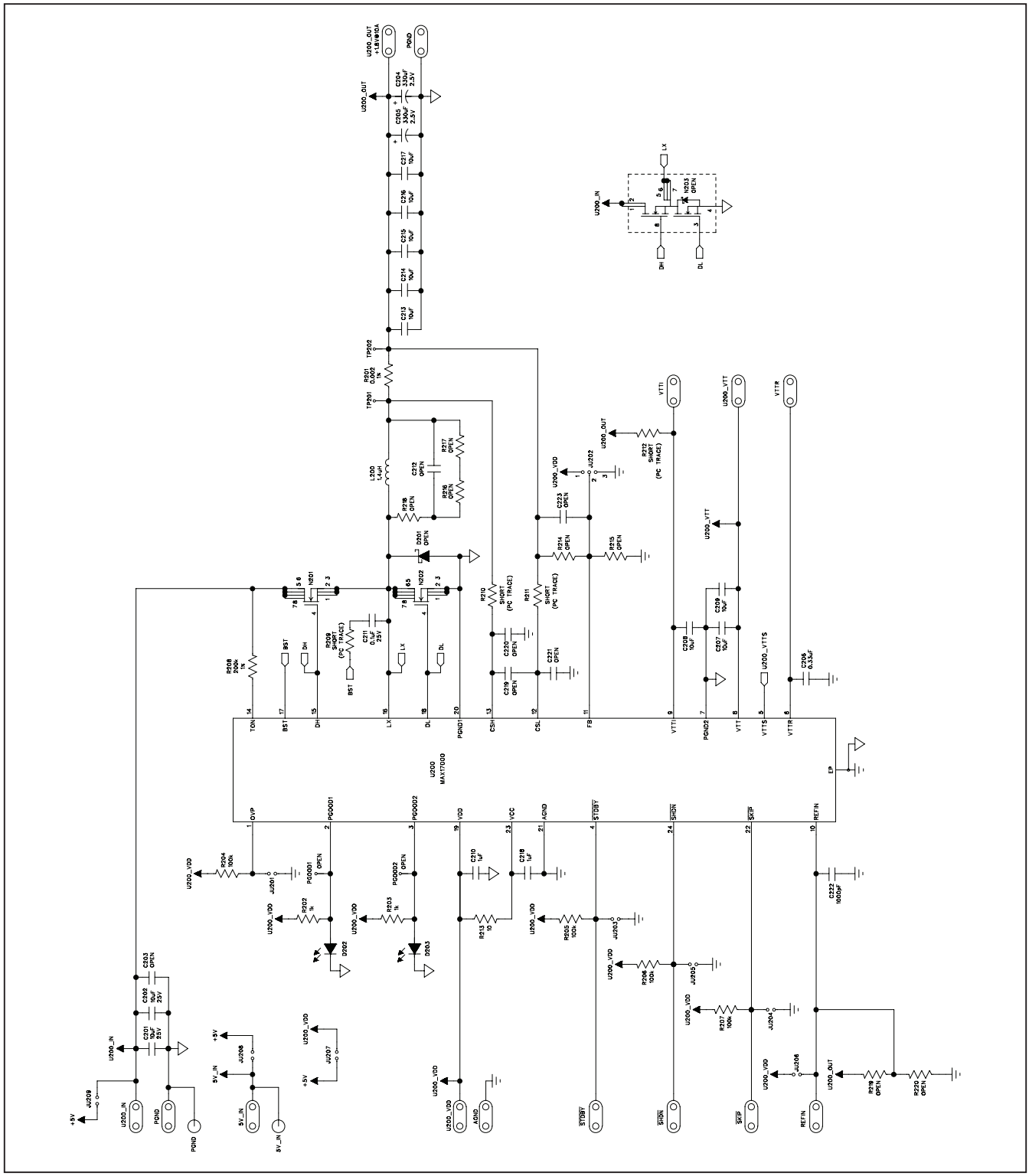

Figure 5c. MAX9530 EV Kit Schematic (Sheet 3 of 13)

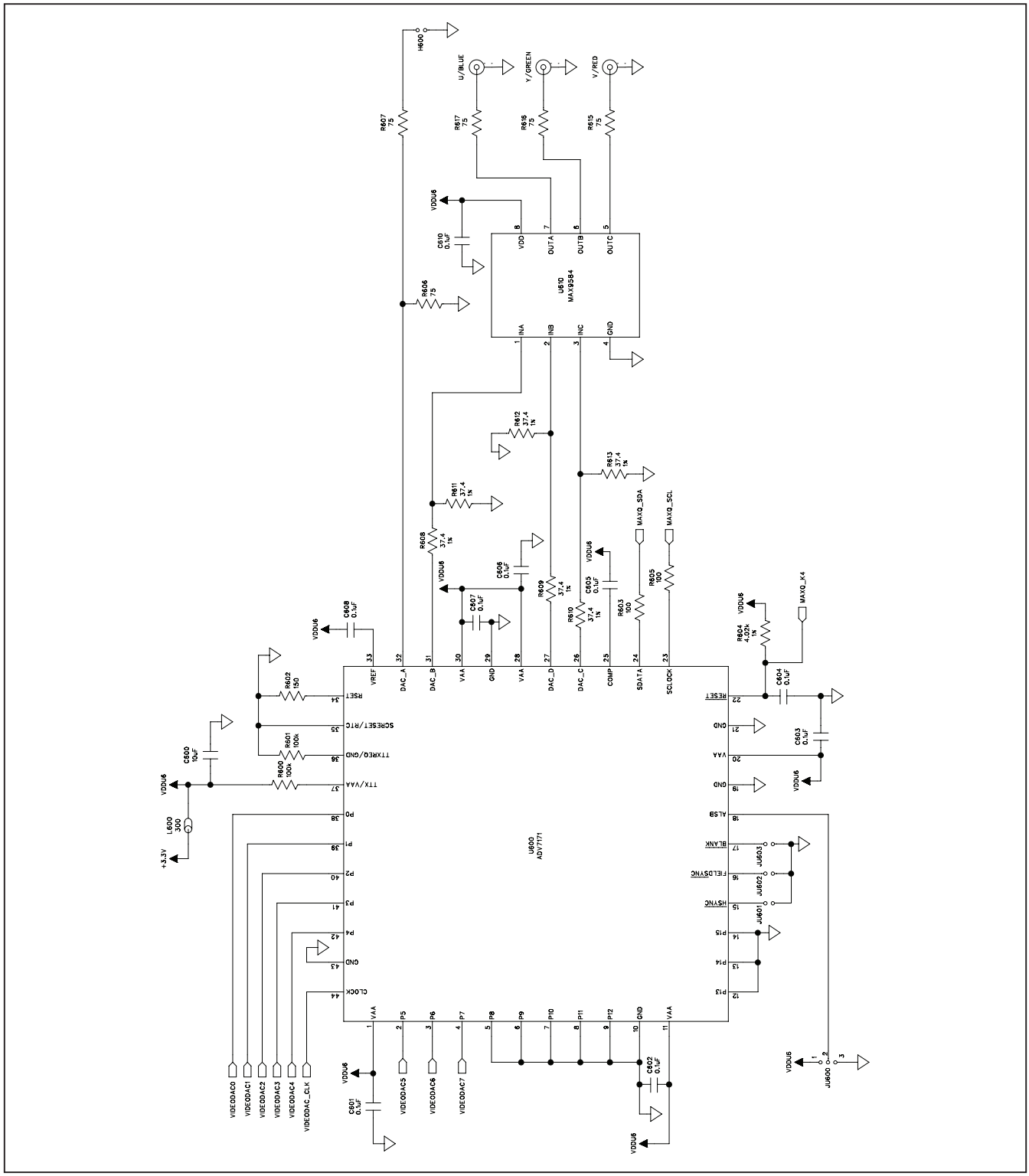


*Figure 5d. MAX9530 EV Kit Schematic (Sheet 4 of 13)*

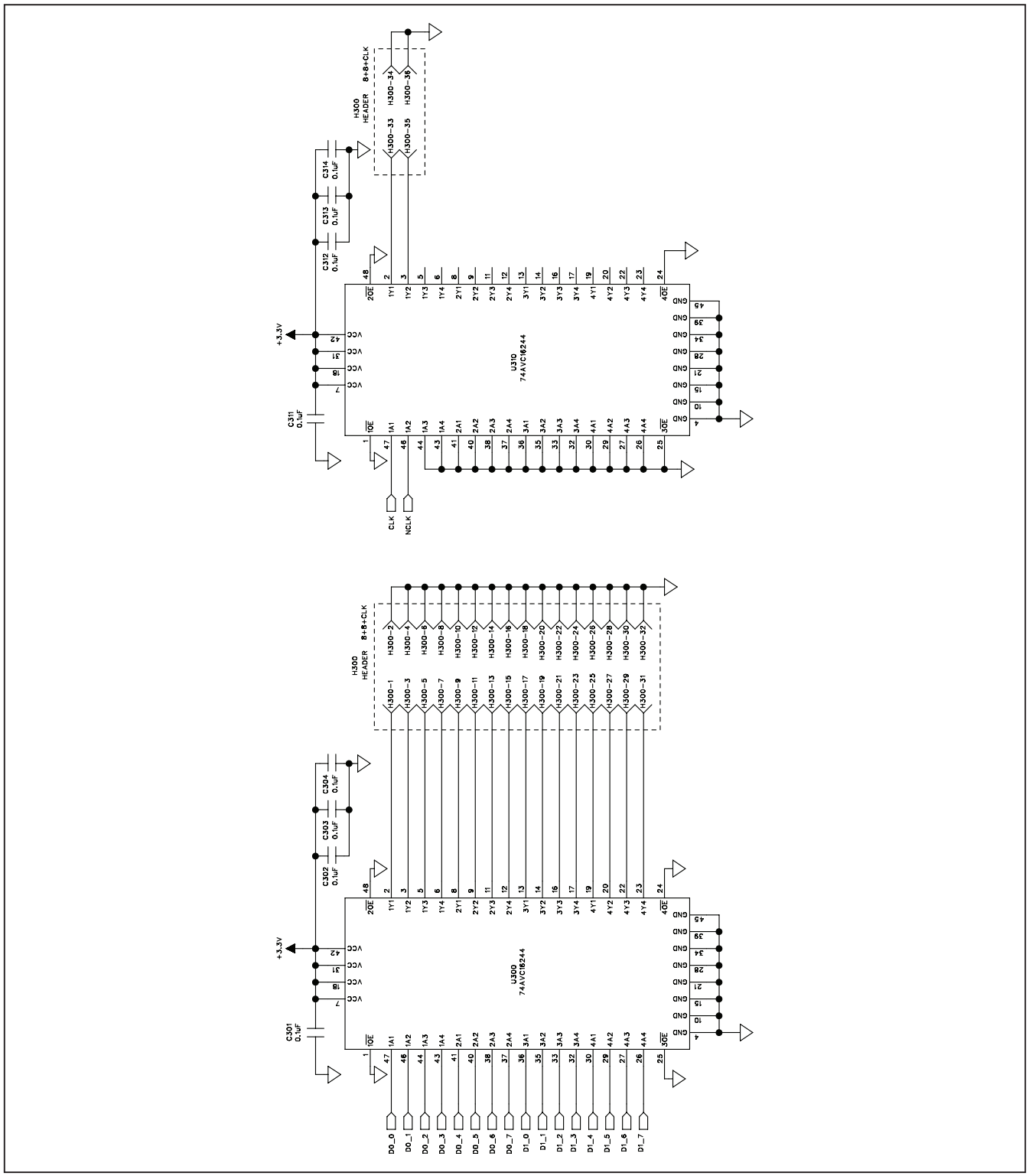


*Figure 5e. MAX9530 EV Kit Schematic (Sheet 5 of 13)*

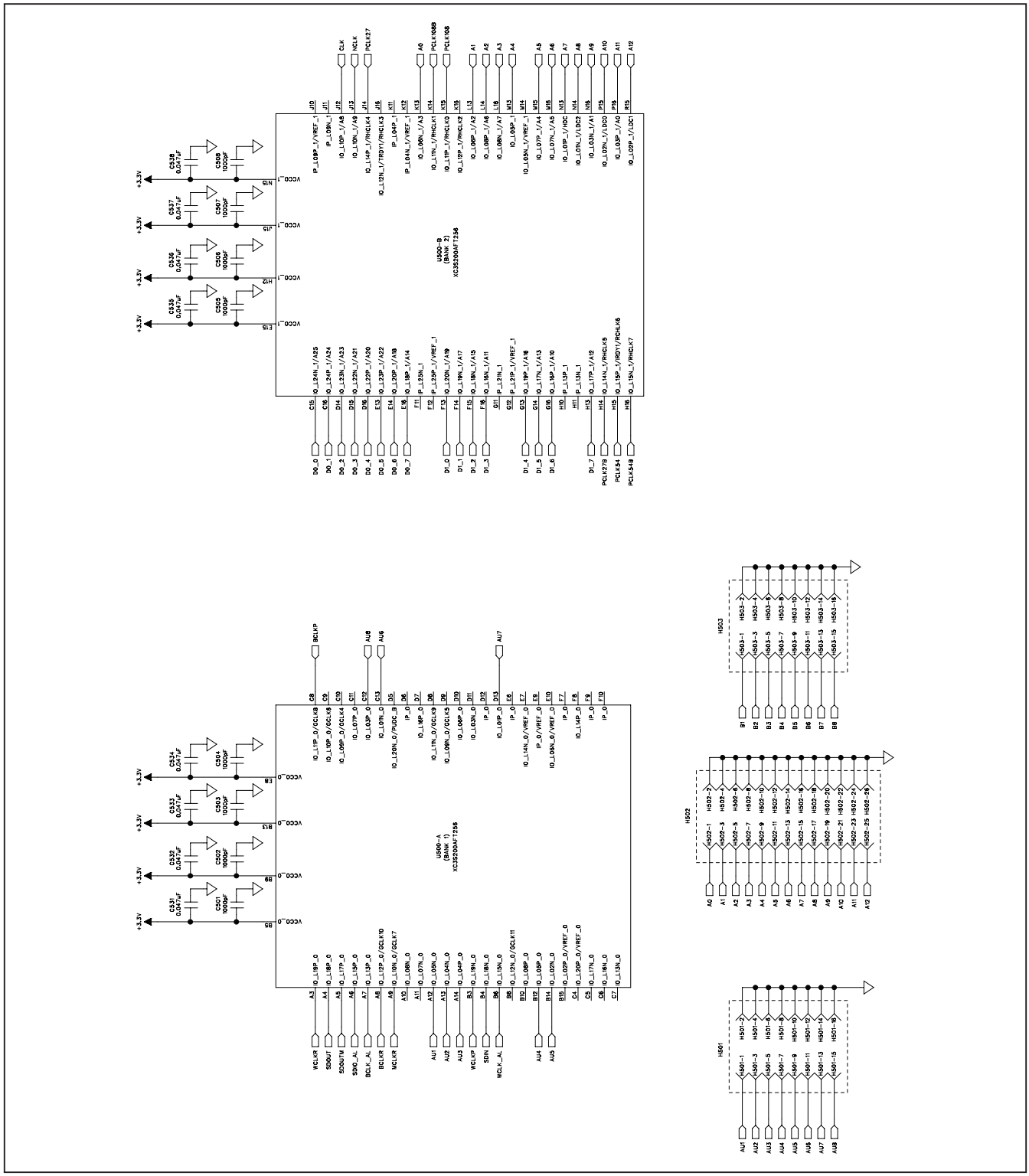

*Figure 5f. MAX9530 EV Kit Schematic (Sheet 6 of 13)*

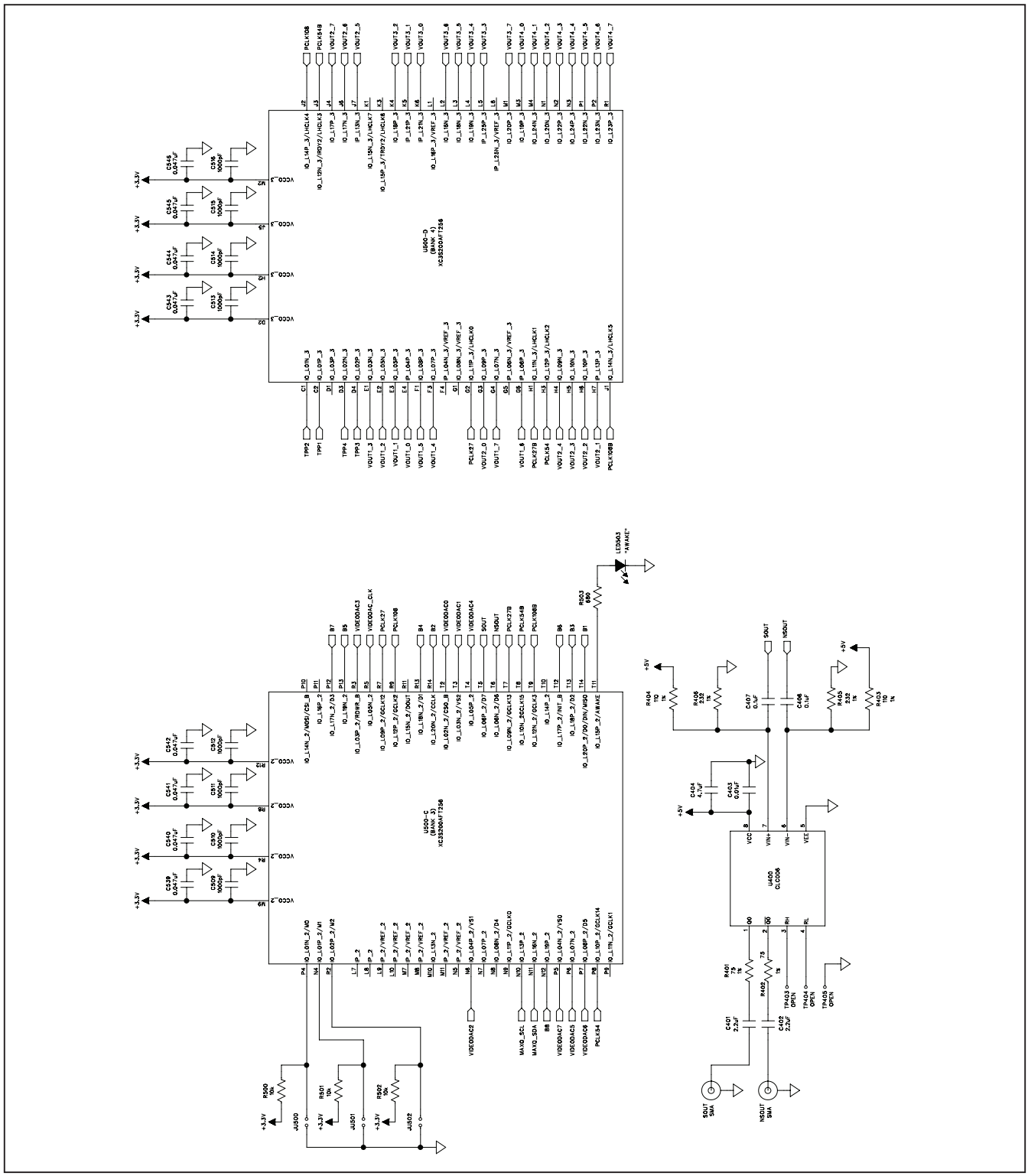

Figure 5g. MAX9530 EV Kit Schematic (Sheet 7 of 13)

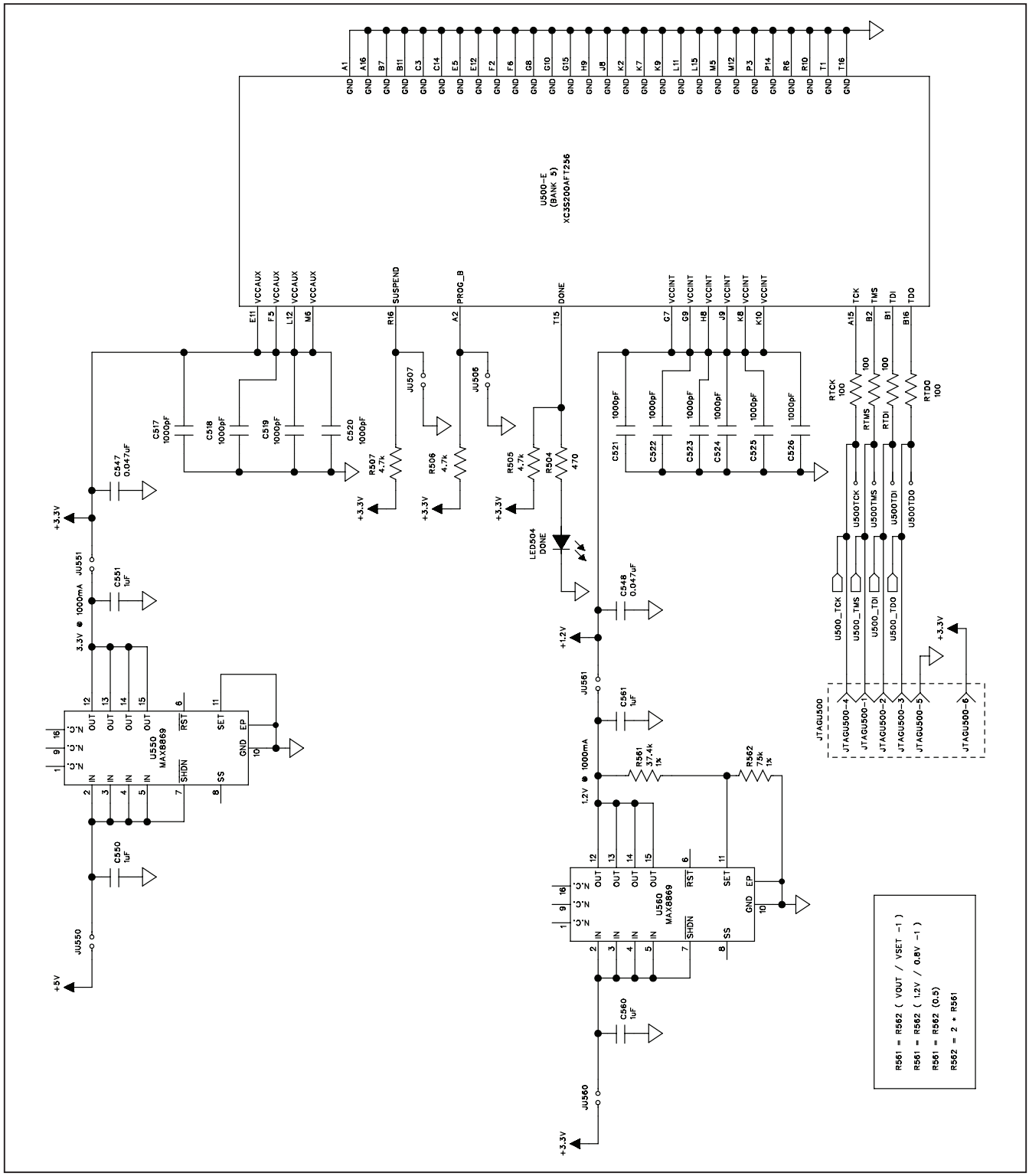


*Figure 5h. MAX9530 EV Kit Schematic (Sheet 8 of 13)*

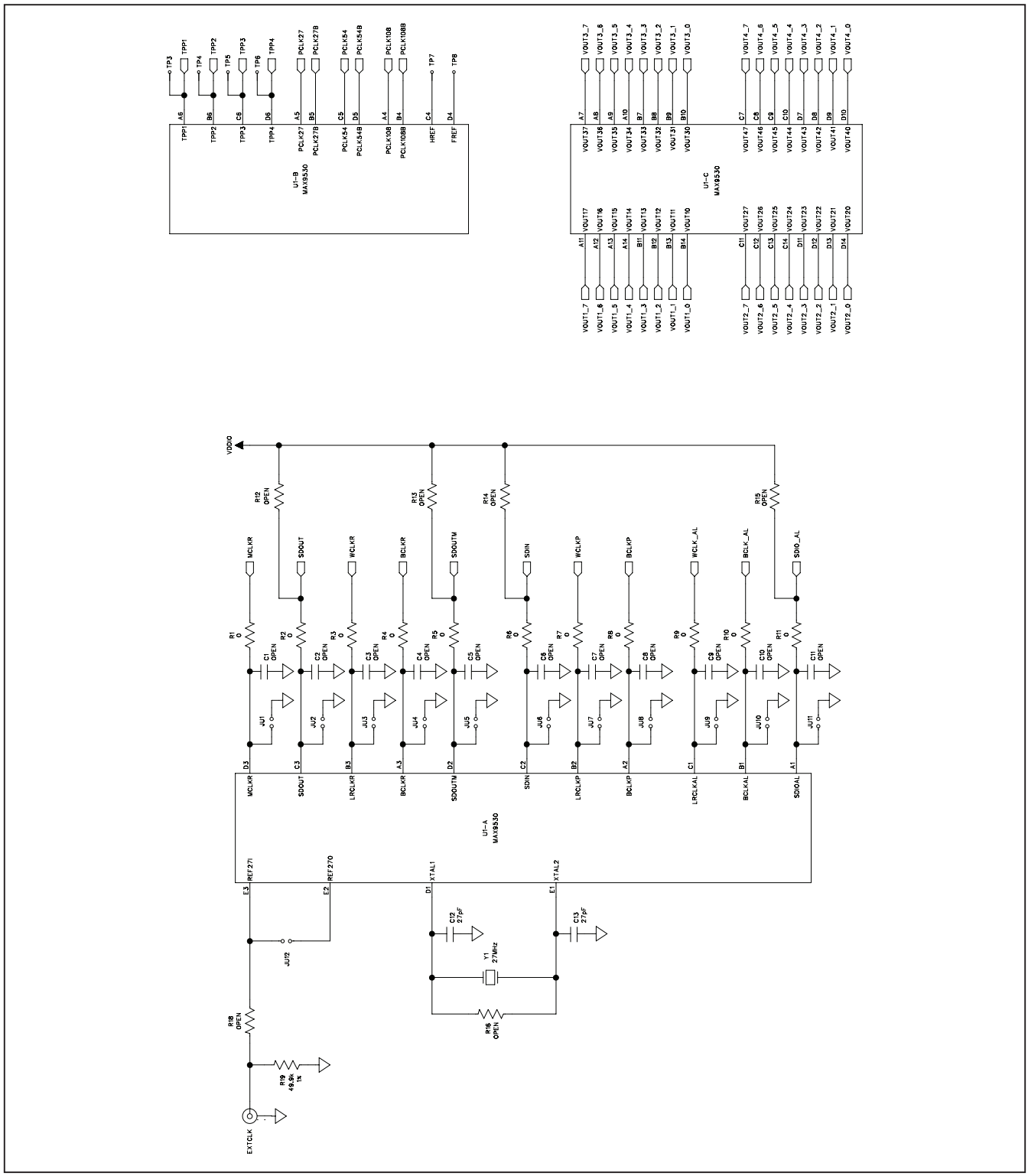

Figure 5i. MAX9530 EV Kit Schematic (Sheet 9 of 13)

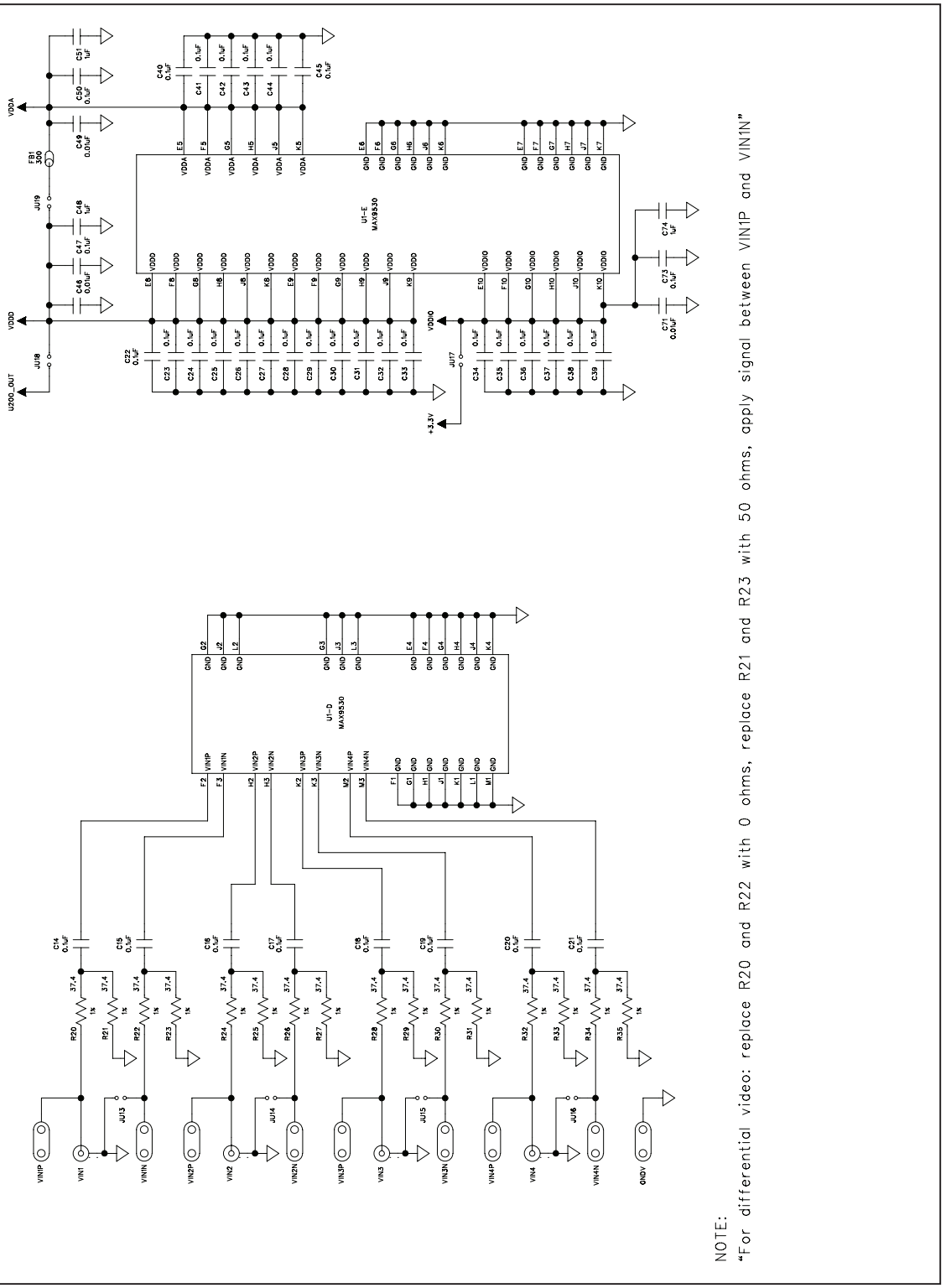


*Figure 5j. MAX9530 EV Kit Schematic (Sheet 10 of 13)*

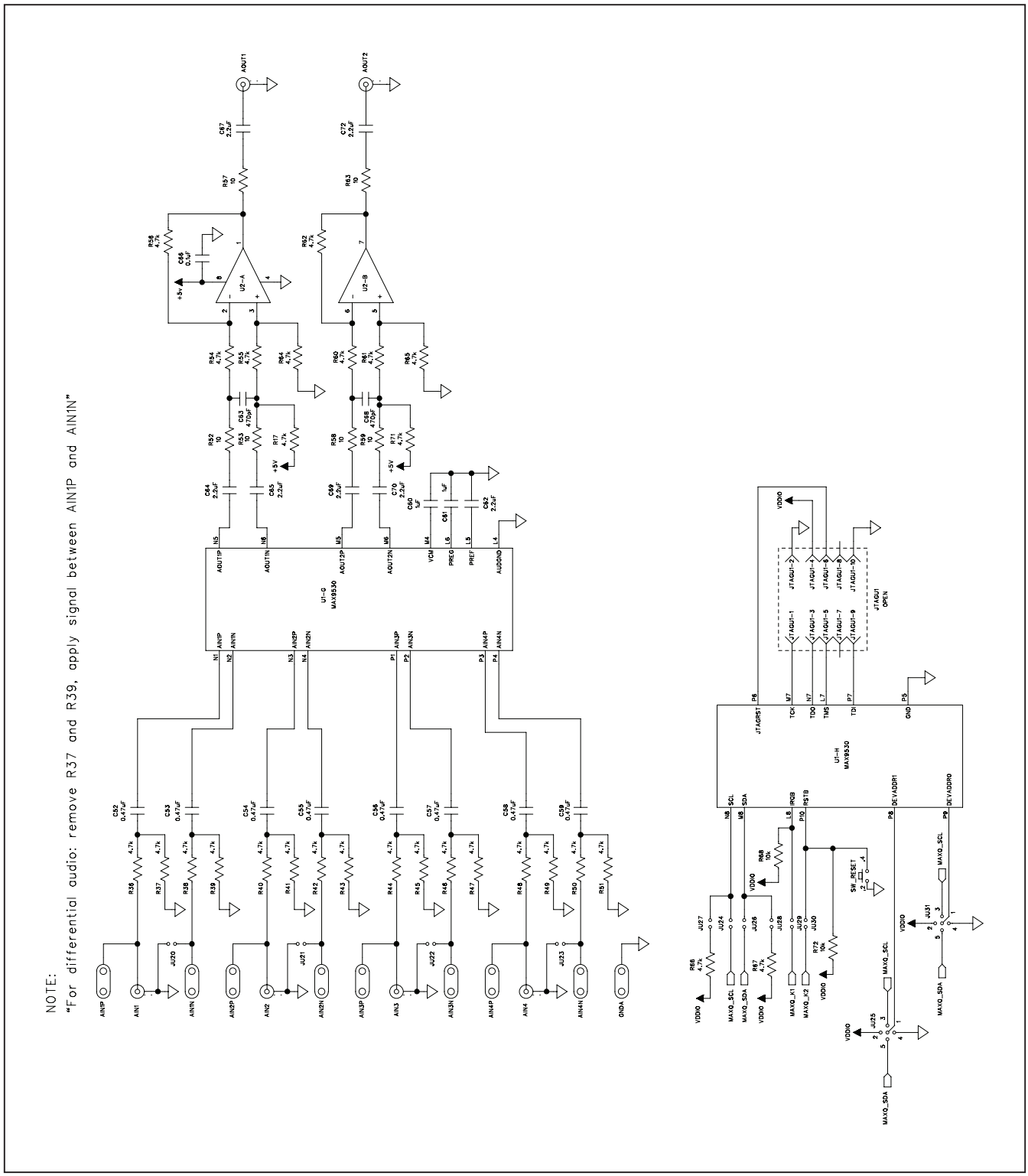


*Figure 5k. MAX9530 EV Kit Schematic (Sheet 11 of 13)*

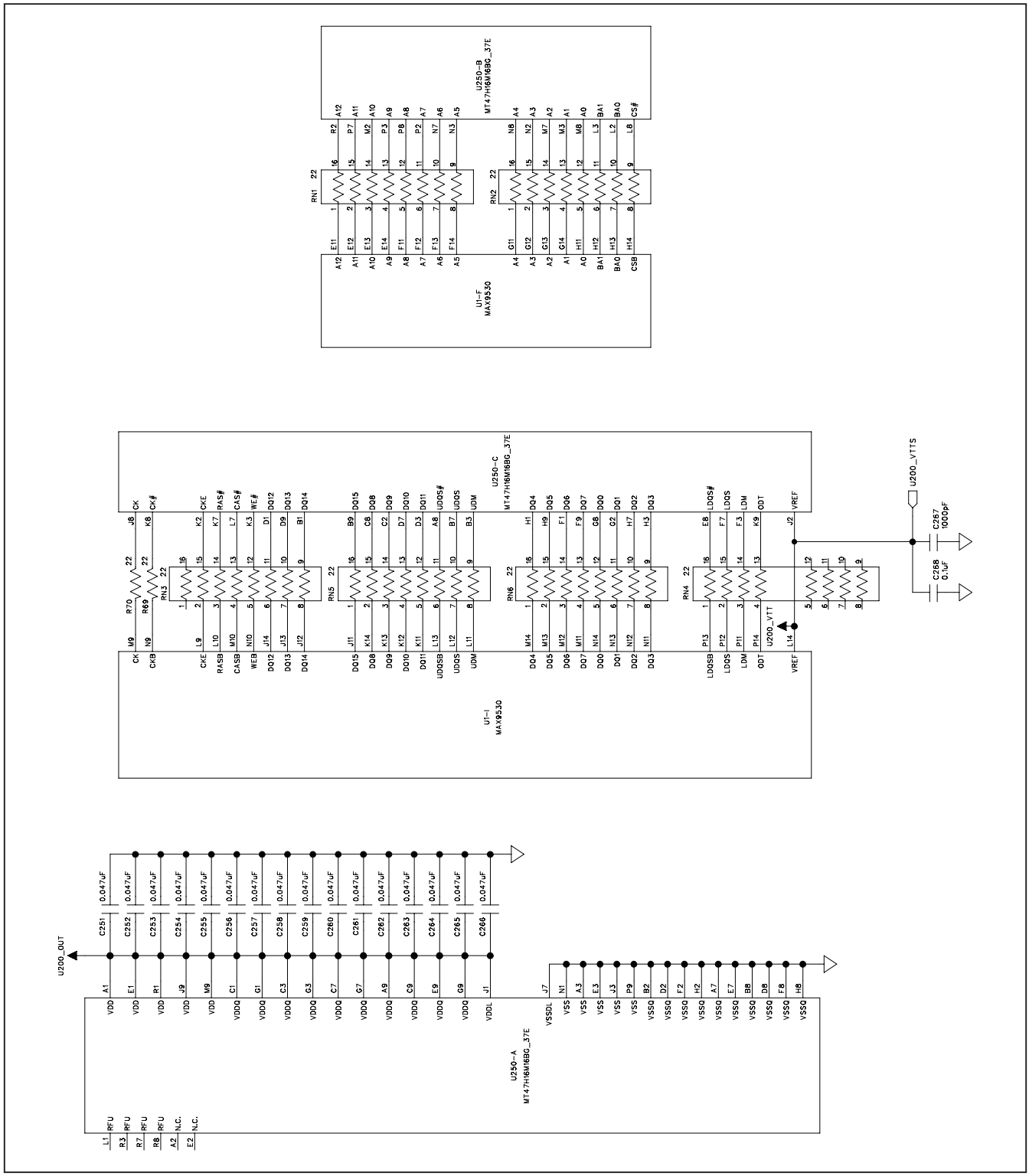

Figure 5I. MAX9530 EV Kit Schematic (Sheet 12 of 13)

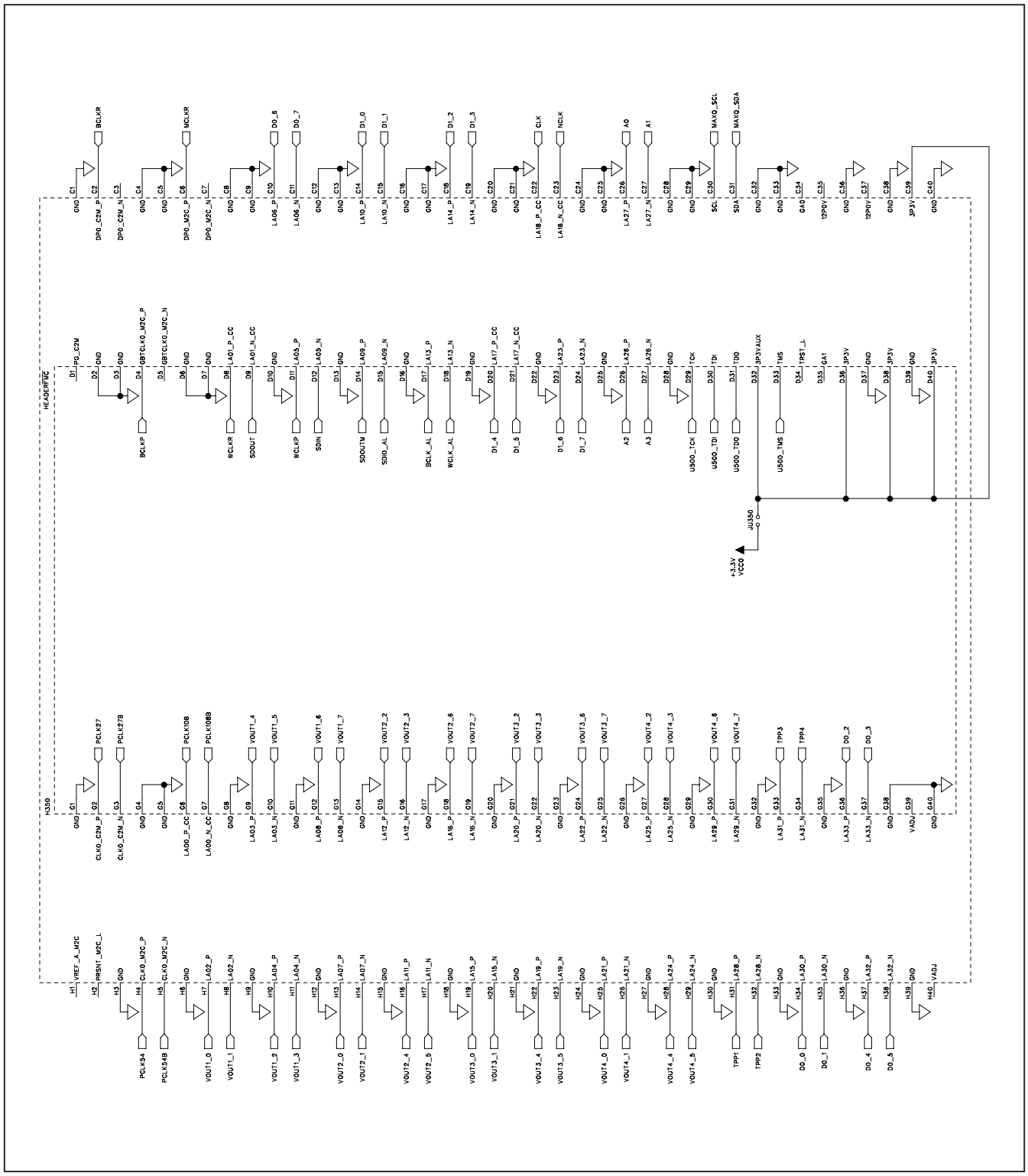

Figure 5m. MAX9530 EV Kit Schematic (Sheet 13 of 13)

# MAX9530 Evaluation Kit

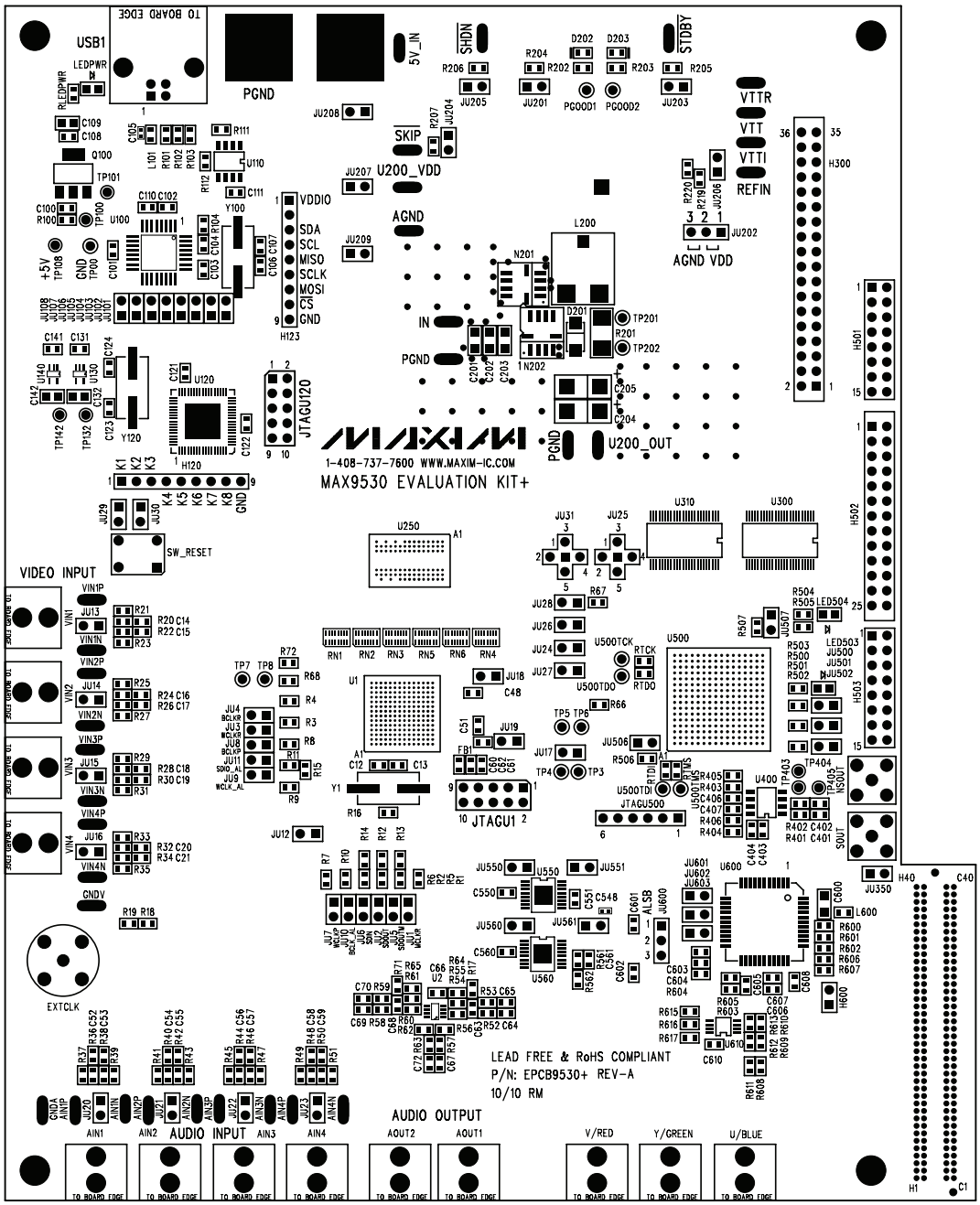


*Figure 6. MAX9530 EV Kit Component Placement Guide—Component Side*

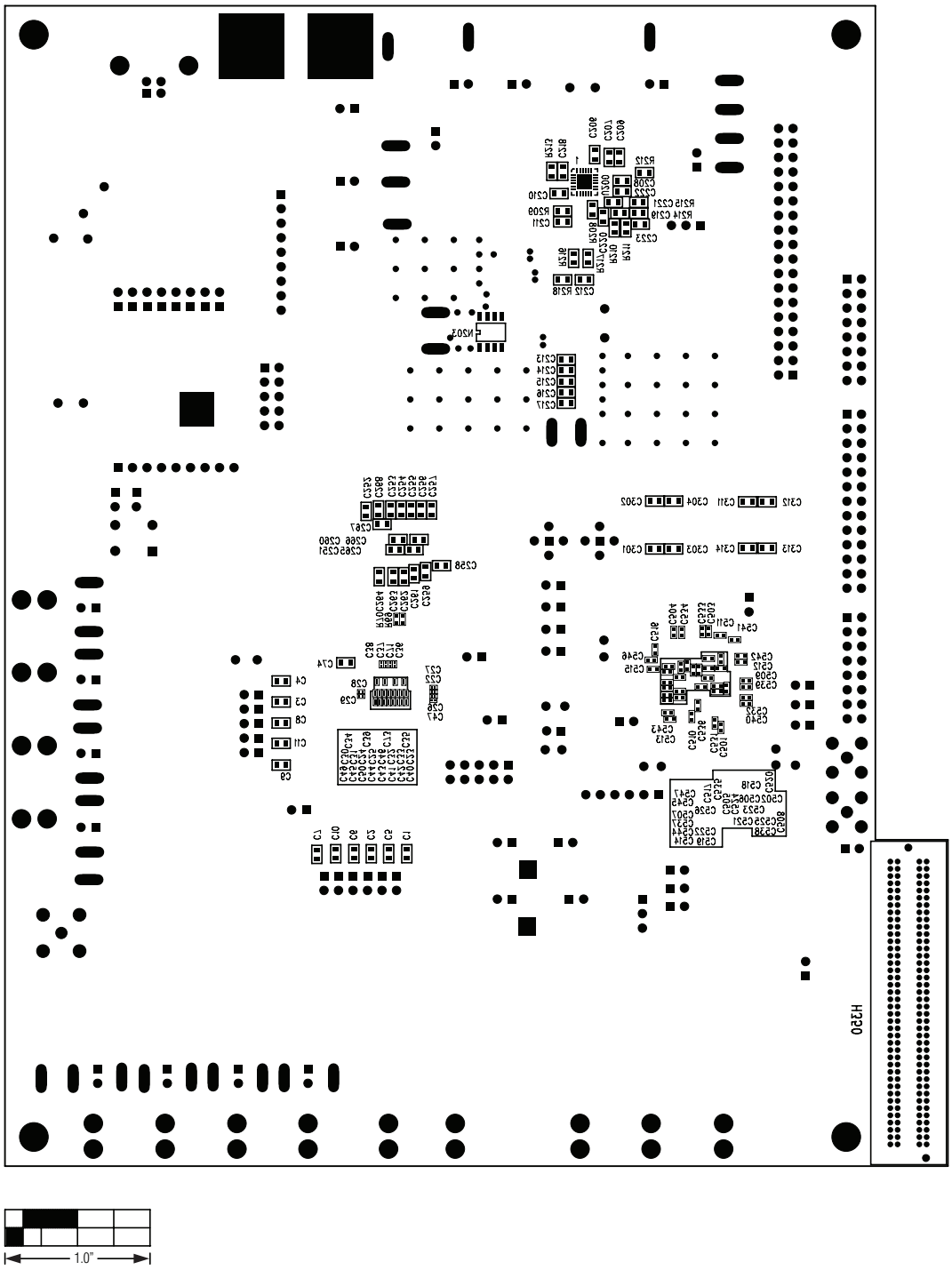


*Figure 7. MAX9530 EV Kit Component Placement Guide—Solder Side*

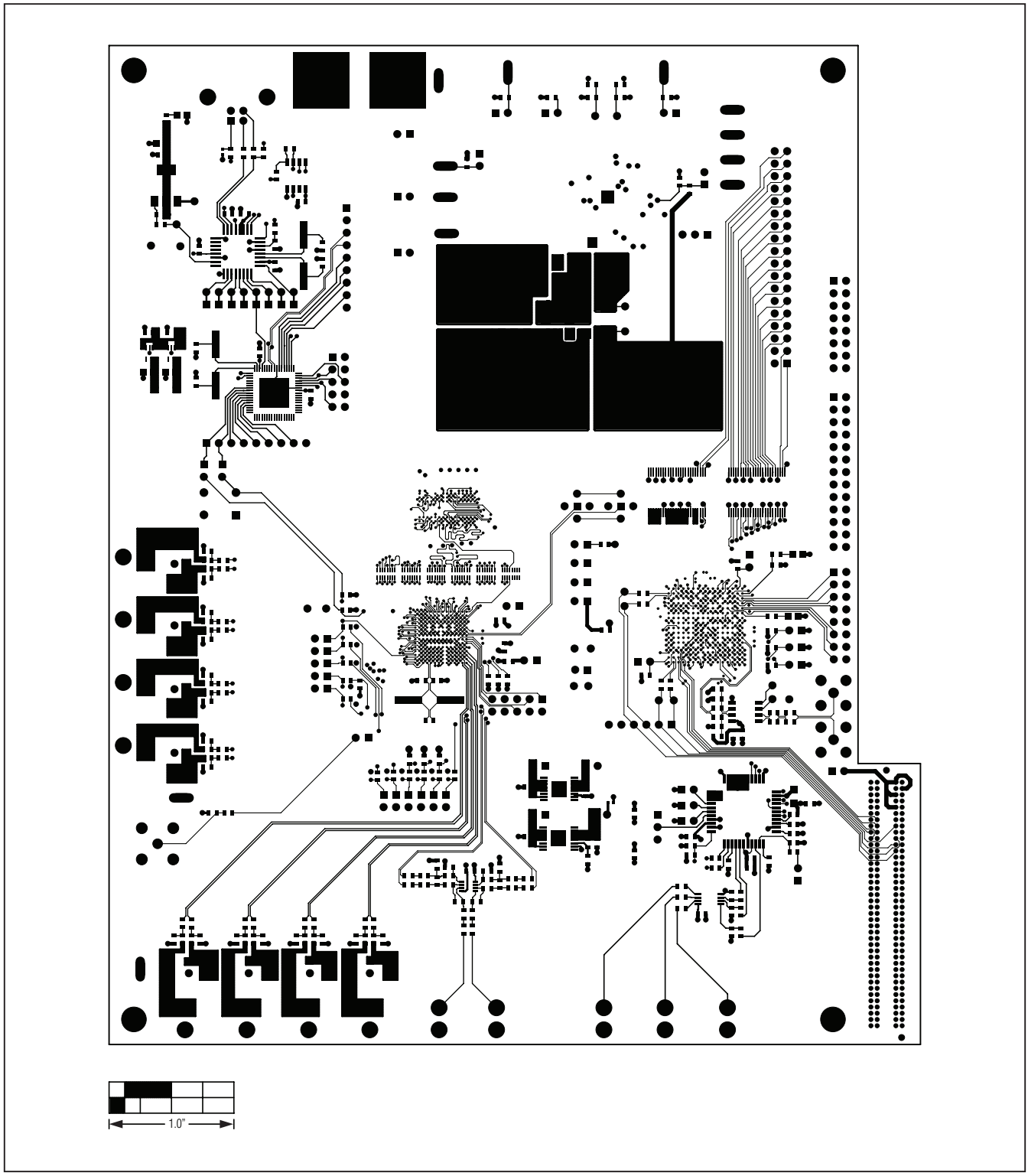


*Figure 8. MAX9530 EV Kit PCB Layout—Component Side*

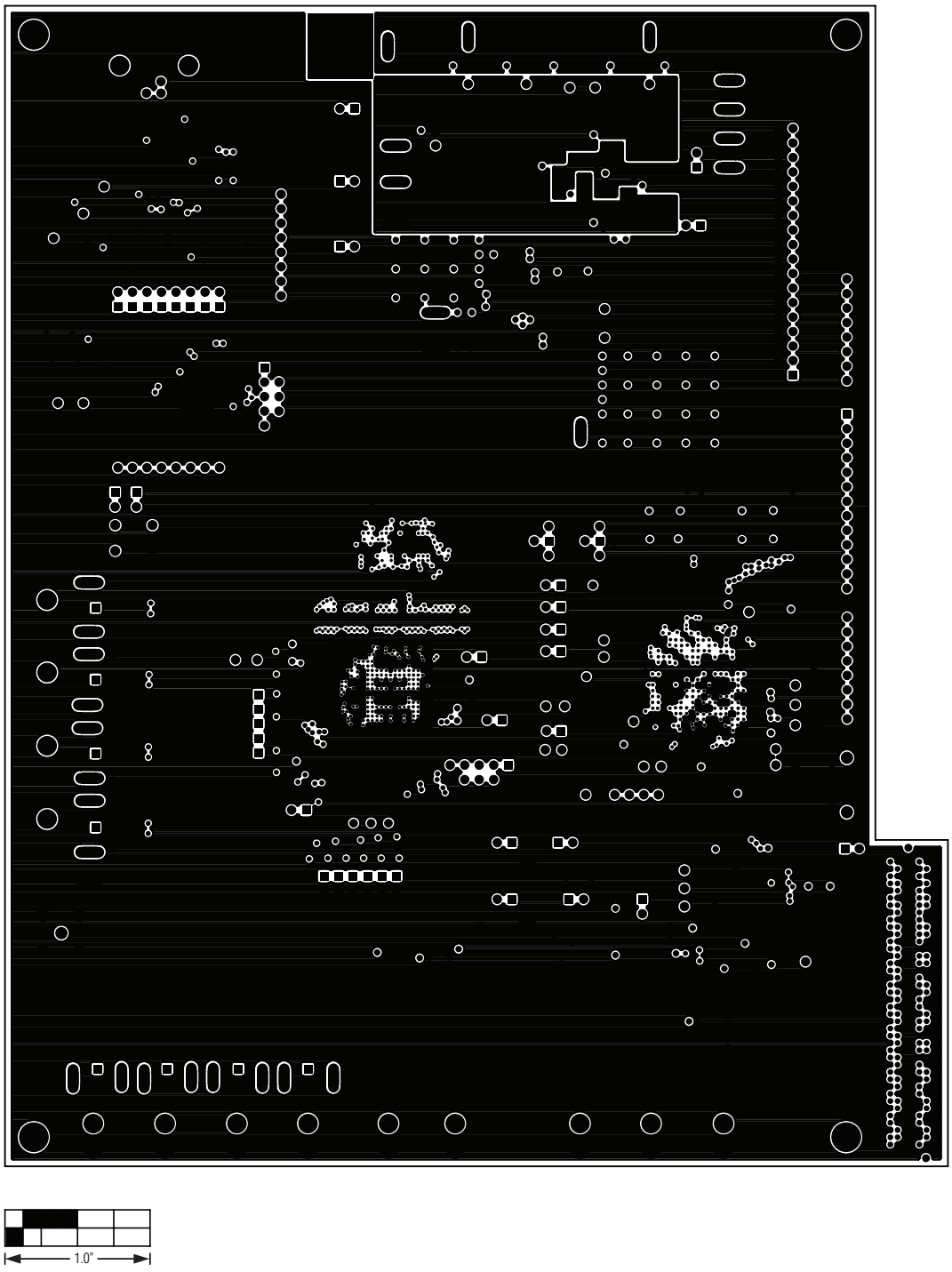


Figure 9. MAX9530 EV Kit PCB Layout—Ground Layer 2

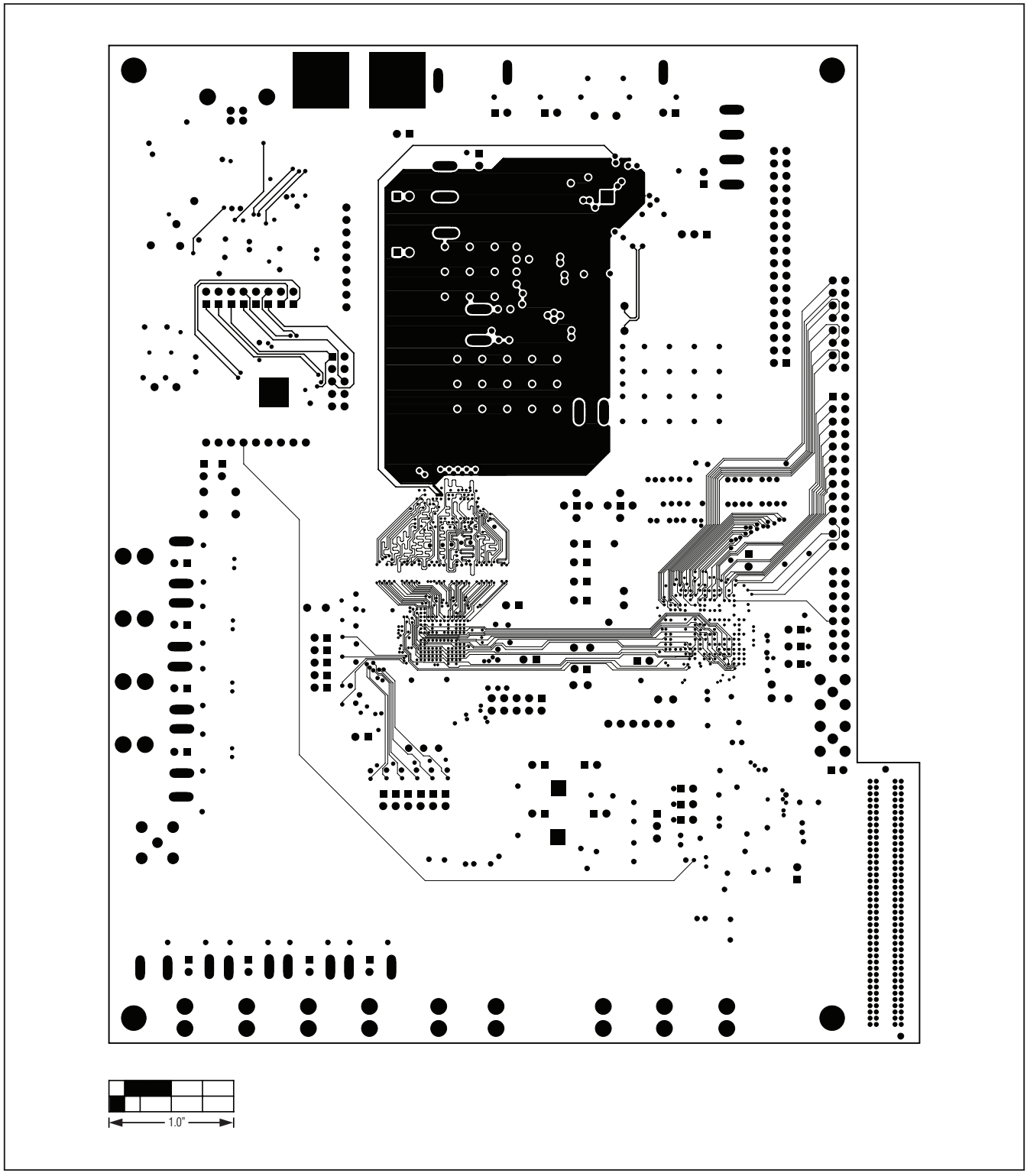


*Figure 10. MAX9530 EV Kit PCB Layout—Power Layer 3*

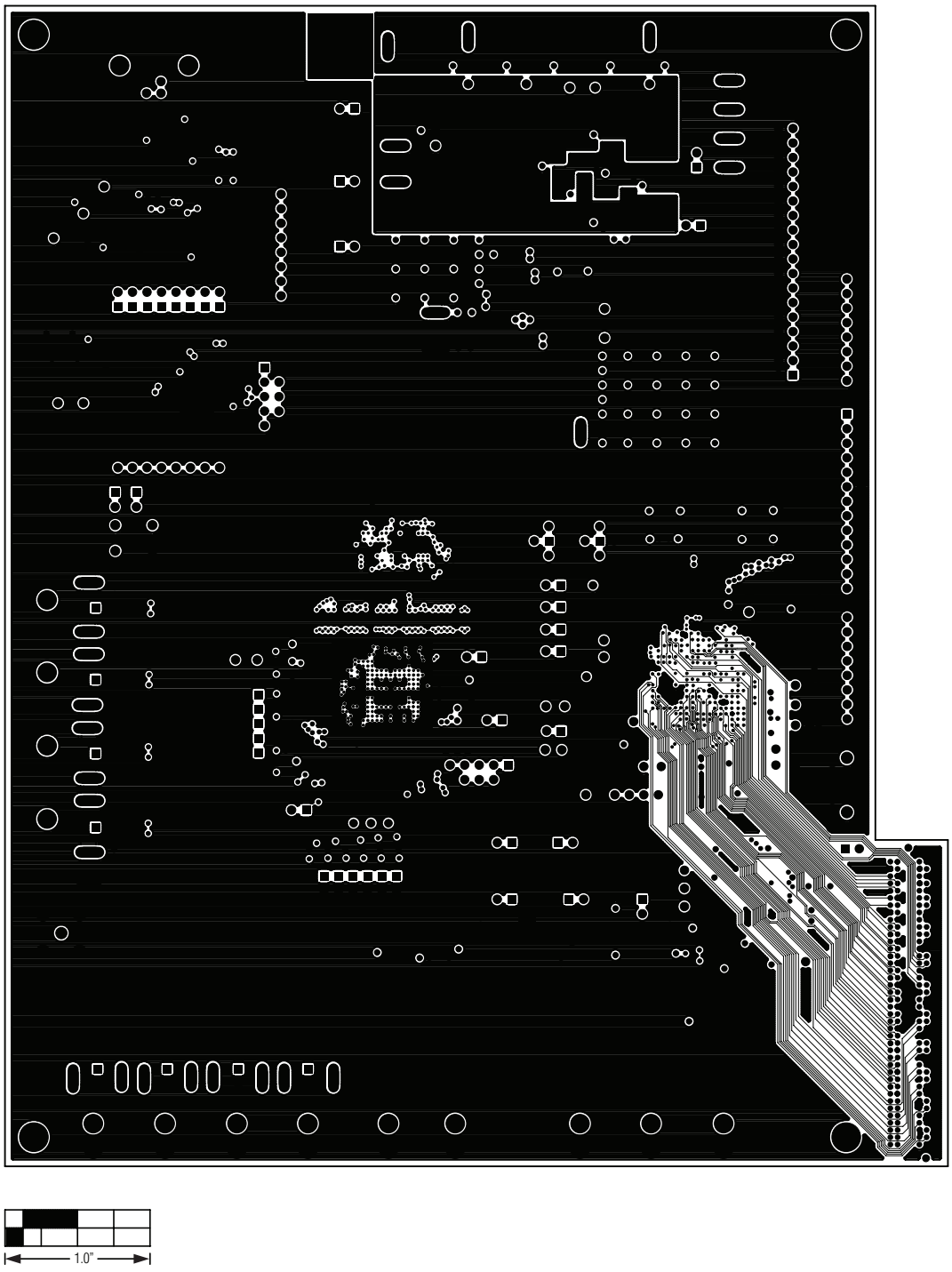


*Figure 11. MAX9530 EV Kit PCB Layout—Layer 4*

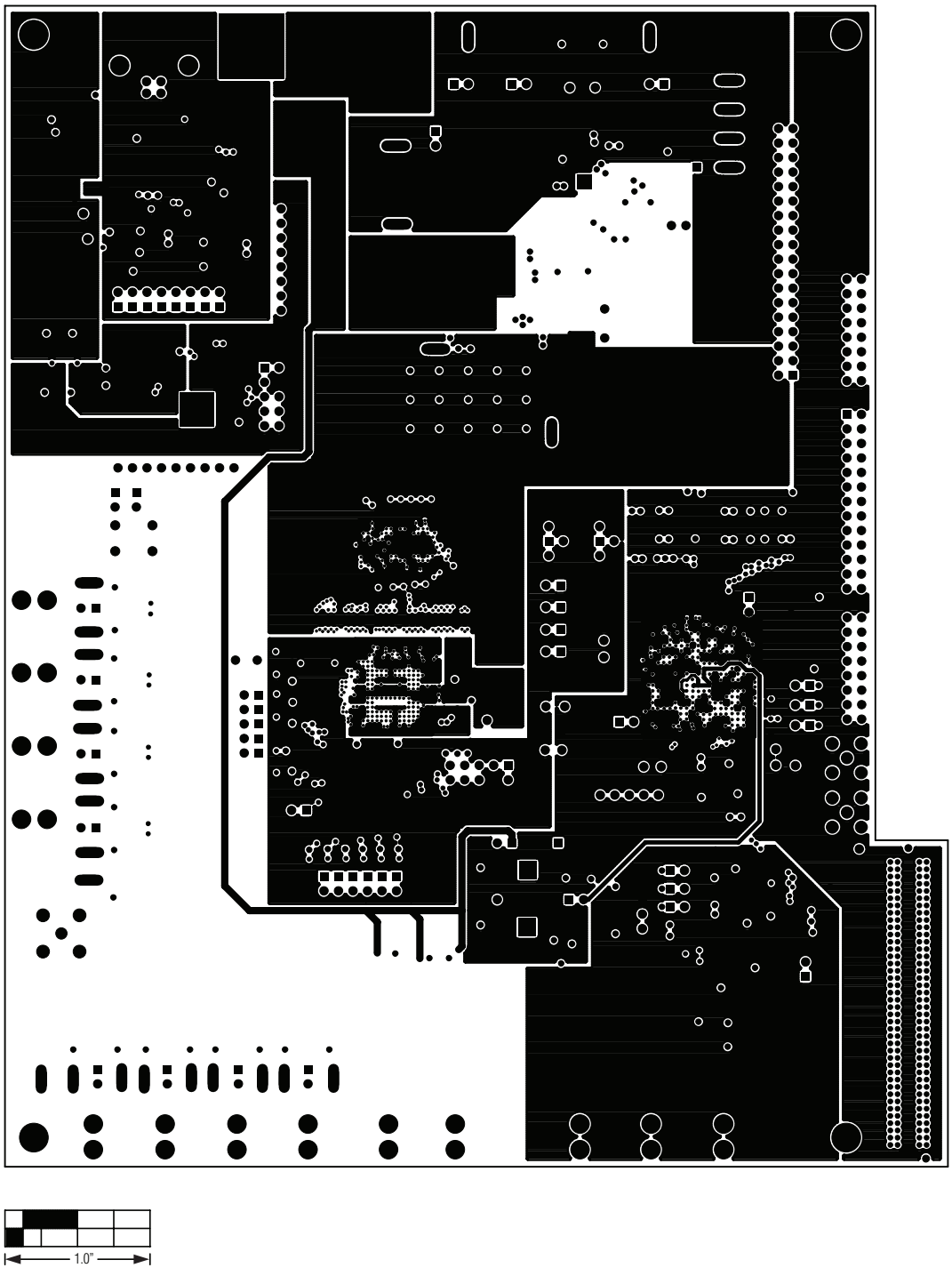


Figure 12. MAX9530 EV Kit PCB Layout—Layer 5

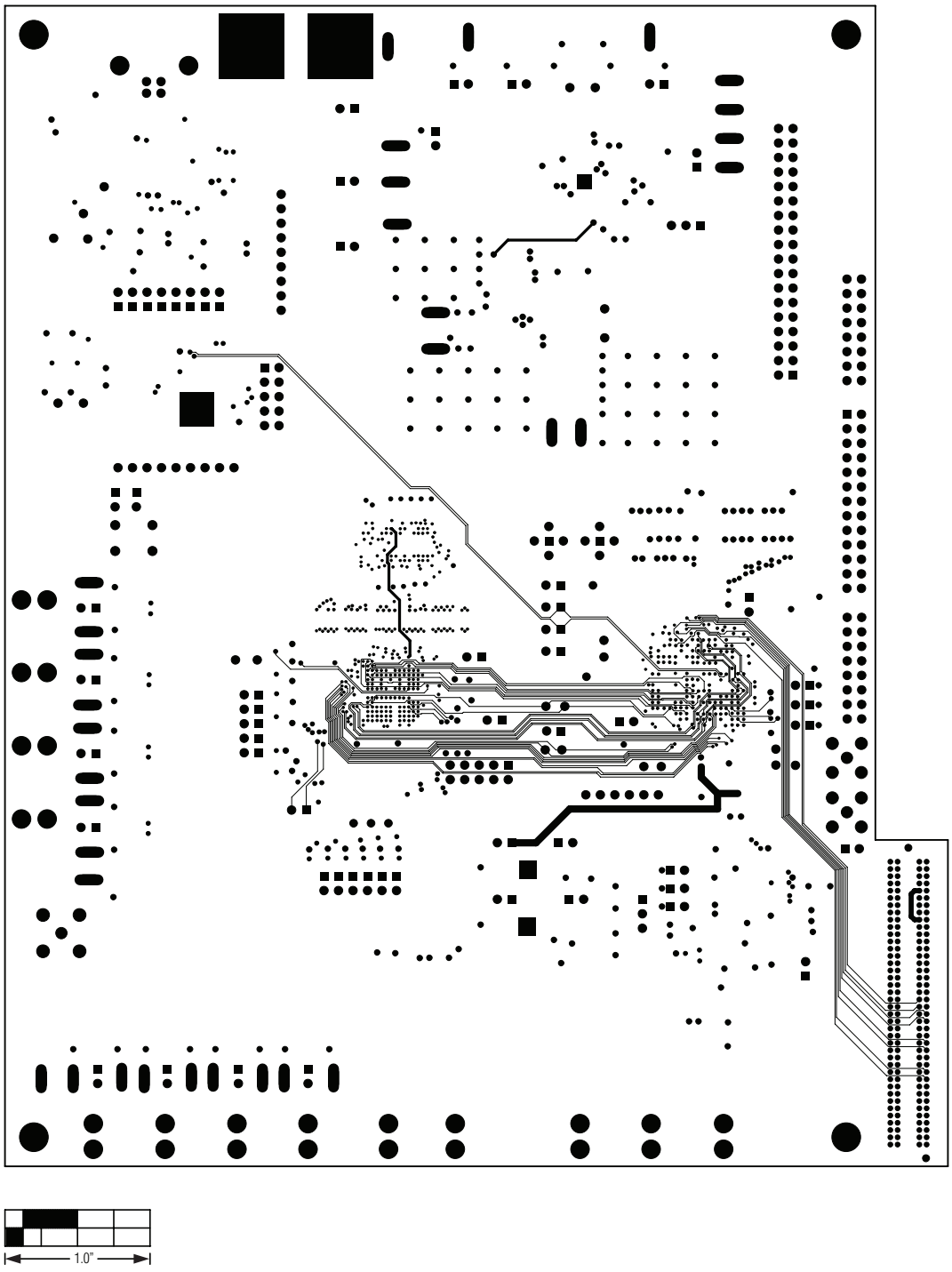


*Figure 13. MAX9530 EV Kit PCB Layout—Layer 6*

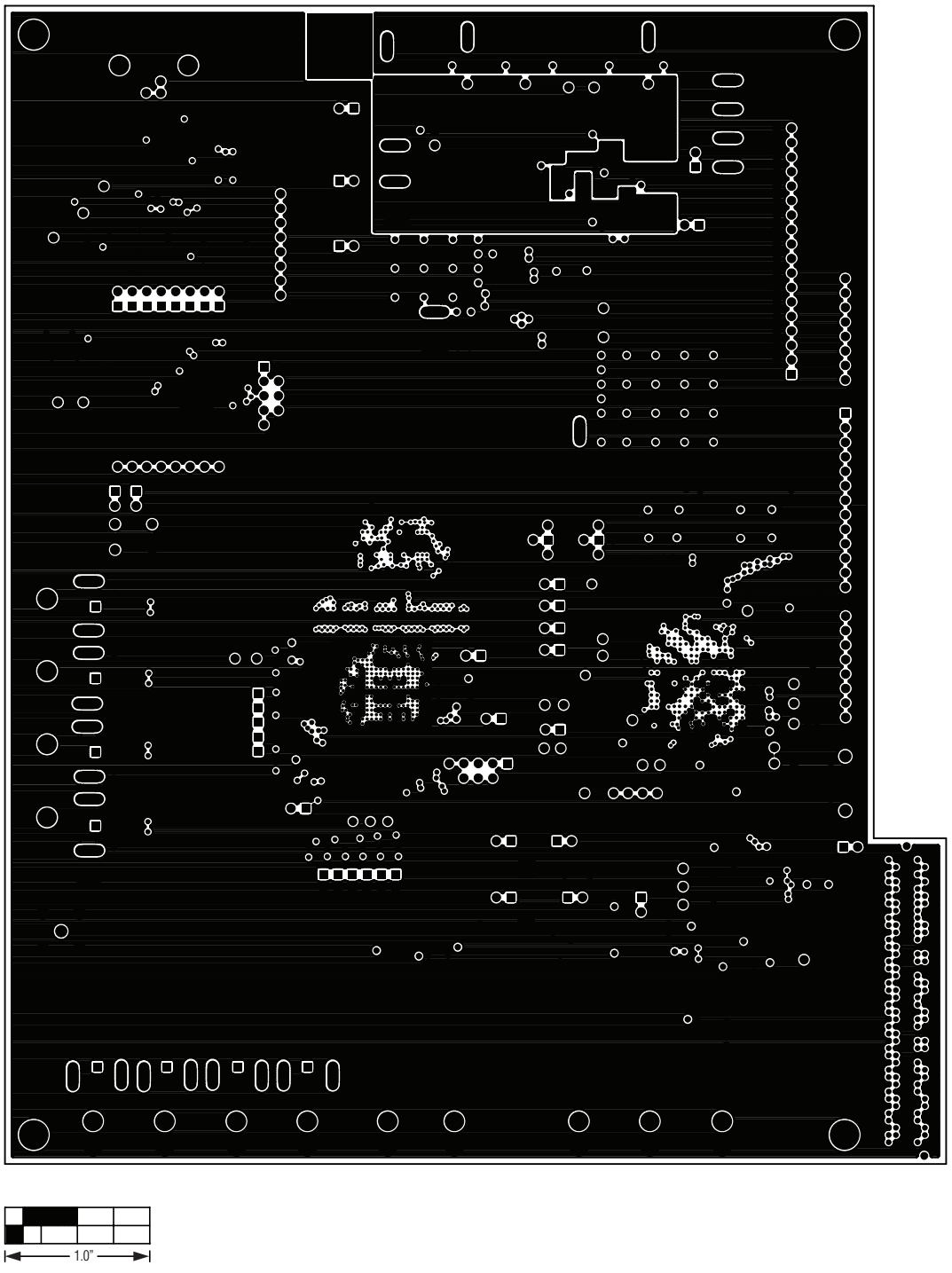


Figure 14. MAX9530 EV Kit PCB Layout—Layer 7

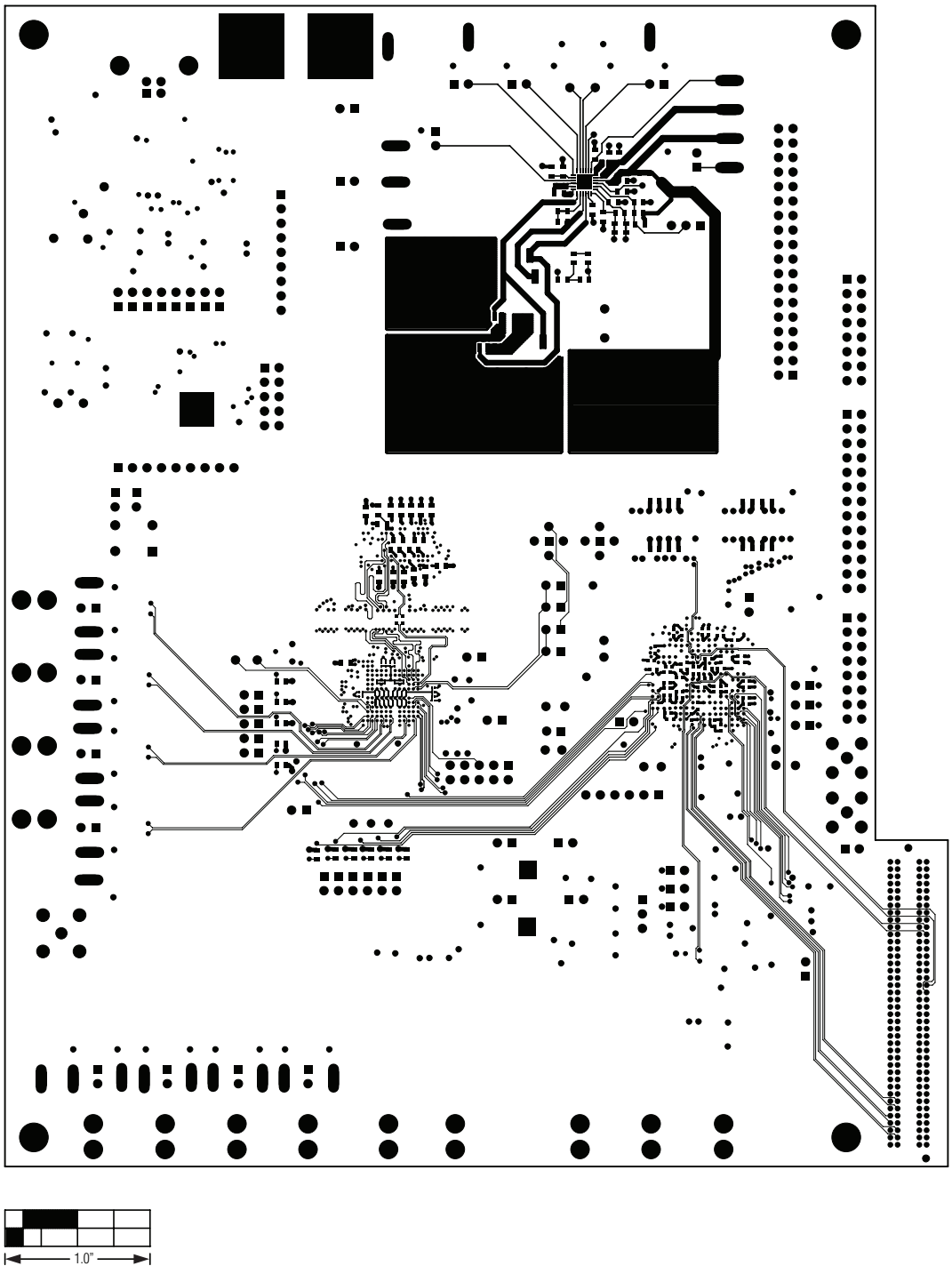


*Figure 15. MAX9530 EV Kit PCB Layout—Component Side*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 12/10 | Initial release | — |